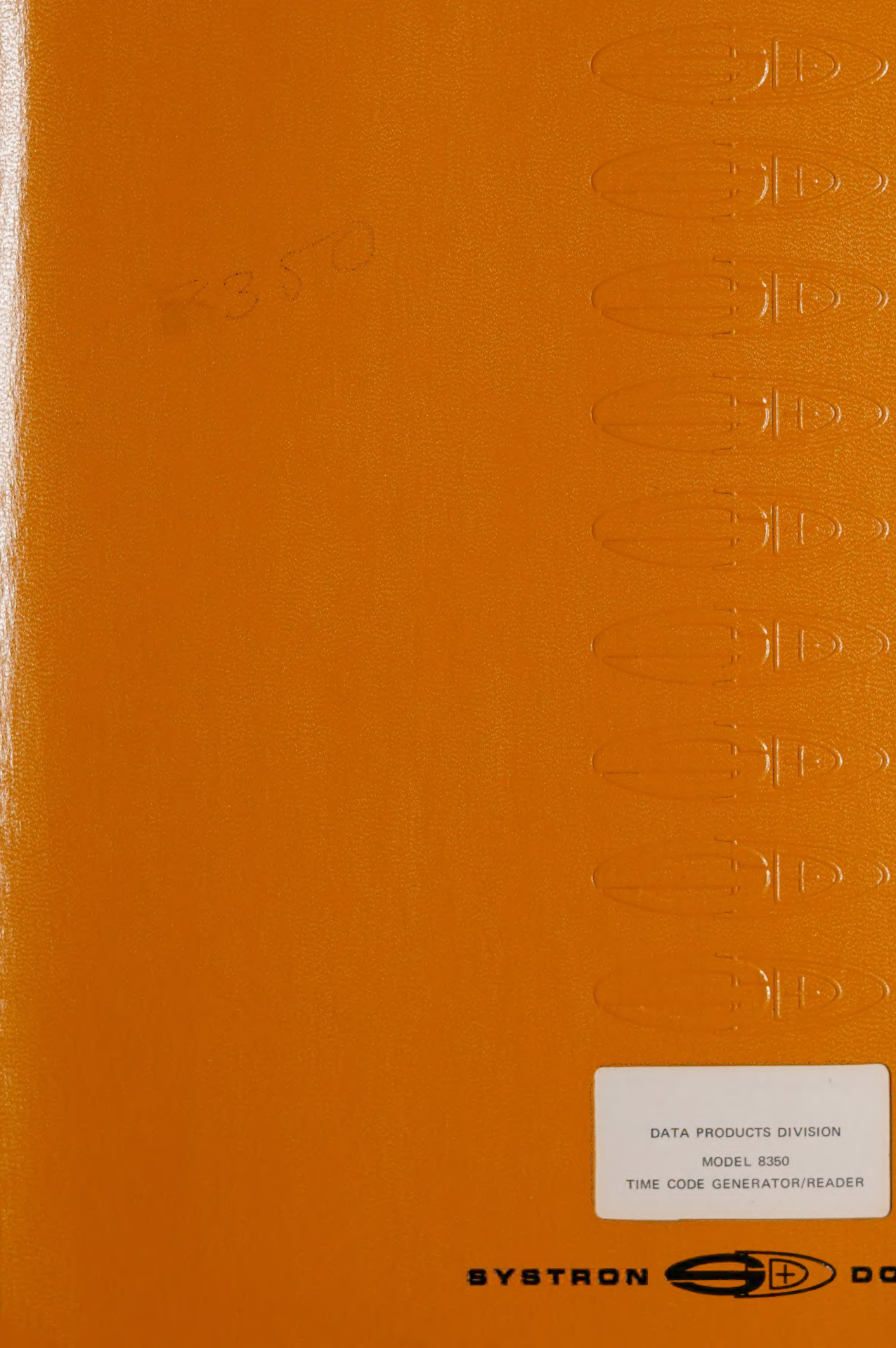

DATA PRODUCTS DIVISION

MODEL 8350

TIME CODE GENERATOR/READER

SYSTRON DONNER

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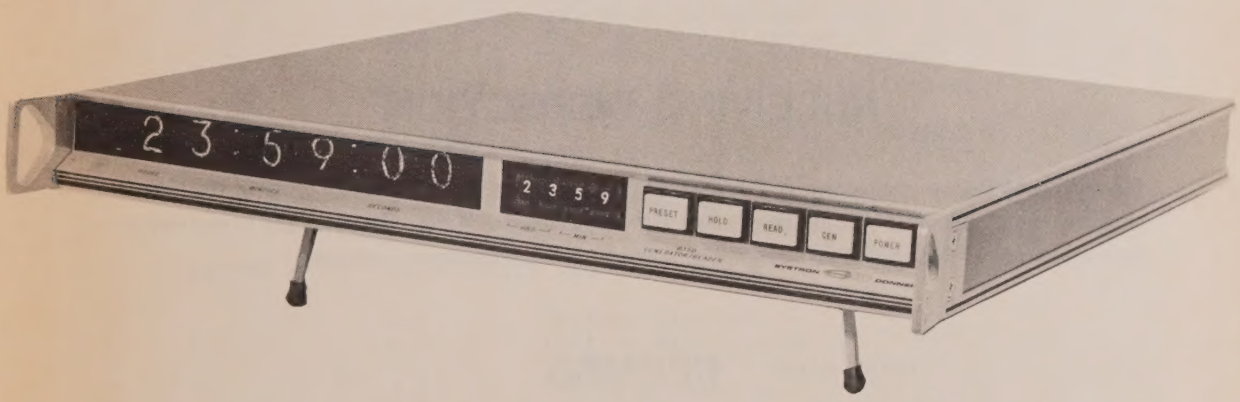


DATA PRODUCTS DIVISION

MODEL 8350

TIME CODE GENERATOR/READER

SYSTRON DONNER
CORPORATION

# WARRANTY

Systron-Donner instruments are warranted during a period of one year from date of shipment to original purchaser to be free from defects in material and workmanship. This warranty does not apply to vacuum tubes, except as these are warranted by tube manufacturers. The liability of Seller under this warranty is limited to replacing or repairing any instrument or component thereof which is returned by Buyer, at his expense, during such period and which has not been subjected to misuse, neglect, improper installation, repair, alteration, or accident. Seller shall have the right to final determination as to the existence and cause of a defect. In no event shall Seller be liable for collateral or consequential damages. This warranty is in lieu of any other warranty, expressed, implied, or statutory; and no agreement extending or modifying it will be binding upon Seller unless in writing and signed by a duly authorized officer.

# RECEIVING INSPECTION

Every Systron-Donner instrument is carefully inspected and is in perfect working order at the time of shipment. Each instrument should be checked as soon as received. If the unit is damaged in any way, or fails to operate, a claim should immediately be filed with the transportation company.

# REPAIRS

Whenever a Systron-Donner instrument requires service, the nearest Systron-Donner representative should be contacted; all representatives will provide immediate service or arrange factory returns when necessary.

Please specify both model and serial number in all correspondence concerning Systron-Donner instruments. Address all inquiries on operation or applications to your nearest sales representative; or, Sales Manager, Concord Instrument Division, Systron-Donner Corporation, 10 Systron Drive, Concord, California 94518.

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CHAPTER 7

Chapter 7 is reserved for information concerning any optional features which have been incorporated into this instrument. If any options are incorporated, the Table of Contents for the optional features will be found at the front of the manual.

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# CHAPTER 1
# CHARACTERISTICS

## 1.1 BASIC FUNCTIONS

The Model 8350 will generate or read a serial modulated time code (generally IRIG B, XR 3 is optional) for use with various recording media. The Model 8350 is commonly used for real time data indexing, access and identification.

### 1.1.1 Generate Function

As a time code generator, the Model 8350 functions as a precise digital clock which produces a coded time signal for recording on magnetic tape as a continuous time reference. The initial start time may be preset in order to record either time-of-day or elapsed time. The time information within the code is in terms of hours, minutes, and seconds. This information is updated each second. Normally the time code is recorded on a separate track of magnetic tape utilizing a direct Record/Reproduce channel. The time code can also, incorporating multiplex techniques, be recorded on the same tape track as the test data.

### 1.1.2 Read Function

As a time code reader, the Model 8350 will monitor a tape's reproduced code during playback and continuously display the received, decoded time information

Two noteworthy monitor circuits are AGC and Error Bypass. An extended range input amplifer coupled with the AGC network accepts an incoming code, 50 Hz to 250 kHz. These large ranges are especially important when scanning the tape at high speed in order to locate a specific time or when reproducing data at faster or slower speeds than that at which it was recorded. The built-in Error Bypass circuitry enables the Model 8350 to disregard up to three consecutive noisy or garbled time frames without losing synchronization. Additionally, the associated digital filtering circuit compensates for brief signal dropouts.

### 1.1.3 Pulse Rate Outputs (Generate and Read Modules)

In addition to the serial time code, the Model 8350 provides four individual, precisely controlled pulse trains of 1000 pps, 100 pps, 10 pps and 1 pps. Since these pulse rates are synchronized with the generated or incoming time code, they may be used for external timing purposes or used to provide time interpolation down to 1 millisecond.

## 1.2 STANDARD FEATURES

In both the generate and read modes,

the updated time is displayed on a six digit, in-line display in terms of hours, minutes and seconds. Lighted colons are provided to separate time increments.

Extreme ease of operation is assured through the use of convenient and simplified control circuitry. Initial time is preset be means of four thumbwheel switches and all operational controls utilize lighted pushbuttons. All signal input and outputs are on quick disconnect BNC type connectors.

With the single exception of the display indicator tubes, all circuitry utilizes proven monolithic integrated circuits and highly reliable, all silicon solid state discrete components. The entire unit is packaged in a light, easy to handle package only 1-3/4 inches high which may be operated in or out of an instrument rack.

## 1.3 SPECIFICATIONS

**Time Base (GENerate Mode):**
Crystal controlled oscillator with a stability of 1 part in $10^5$ per day (0° to 50° C).

**Display (GENerate and READ Modes):**
Six digit in-line readout to indicate time-of-day or elapsed time in hours, minutes and seconds with lighted colons to separate time increments.

**Time Preset:**
Four Thumbwheel switches to preset hours and minutes to desired initial time. Seconds display presets to zero.

**Code Format:**
Modified IRIG B in terms of BCD hours, minutes and seconds.

**Output Code (Generate Mode):**
Carrier Frequency: 1 kHz.
Output Level: Adjustable from 0 to 10 volts peak-to-peak from a low impedance 15 mA peak current source.
Modulation (Mark-to-space): 3:1 (±10%).
Connector: BNC, rear panel.

**Input Code (Read Mode):**
Carrier Frequency: 50 Hz to 250 kHz from controlled or uncontrolled tape speeds.
Direction: Reads code in forward direction only.
Level: 0.25 to 10 volts peak-to-peak. into 250 kΩ, minimum.
Modulation Ratio (Mark-to-space): 2:1 to 6:1.
Connector: BNC, rear panel.

**Pulse Rate Outputs (GENerate and READ Modes):**
Simultaneous pulse rates of 1000 pps, 100 pps, 10 pps and 1 pps are provided.

# IMPORTANT MAINTENANCE INFORMATION
# FOR
# PRINTED-CIRCUIT BOARD REPAIR

*NOTE*

*READ BEFORE CHANGING ANY COMPONENT ON A PRINTED-CIRCUIT BOARD*

Replacing integrated circuits or other electronic components soldered to printed-circuit boards, the procedures indicated below must be followed or damage to the board may result:

1. Determine by troubleshooting techniques, which integrated circuit or discrete component(s) has failed.

2. Remove the defective component(s) from the board by cutting the pins or leads with a small diagonal clipping tool. (Always remove and replace the entire component.)

3. Apply heat (40-50W soldering iron) sparingly to each of the cut pins or leads and remove from the board; clean the hole(s) with a toothpick or solder suction tool.

4. Form the tinned leads of the replacement part and insert in the printed circuit holes; solder, then trim leads to extend 1/16-inch beyond the back surface of the board. (Use only 63-37 solder with maximum 1/16-inch diameter.)

*CAUTION*

*Always trim semiconductor leads only after soldered installation is complete. This procedure greatly lessens the possibility of component failure due to shock-wave damage caused by the trimming tool.*

5. When soldering semiconductor devices and all small components, be sure to use a heat sink tool or long-nosed plier connected to the component lead(s) while each is being soldered. Allow the soldered connection to cool before removing the heat sink.

6. Clean all dirt and solder-flux from the printed circuit traces by liberal application of isopropyl alcohol or freon-type solvents.

Level: 0 to +5 volts, nominal.

Connectors: BNC on rear panel for each rate.

**Environment:**

0° to +50° C at up to 95% relative humidity.

**Power:**

117/230 volts (±10%); 48 to 440 Hz.
30 watts.

**Package:**

1-3/4" high x 19" wide x 20" deep.
Flip down tilt stand for table top operation; rack mount kit for rack mount applications. Net weight: 30 lbs.

## 1.4 STANDARD OPTIONS

**Option A11B:** IRIG B DC Level Shift Output.

**Option A11E:** IRIG E DC Level Shift Output.

**Option A18:** Coincidence Output Signal to allow searching to a selected start time on tape or to actuate relays, alarms, etc.

**Option B16:** High Stability 1 MHz Oscillator 2 x $10^9$/Day and aging rate of 1 part in $10^9$/Day.

**Option C26:** Generates and Reads XR 3 modulated Code (250 Hz) carrier in lieu of IRIG (12, 24, 36 millisecond bit structure).

**Option C26A:** Generates and Reads XR 3 modulated Code (1000 Hz) carrier in lieu of IRIG B (12, 24, 36 millisecond bit structure).

**Option D11N:** Provides 20 lines of BCD outputs (hours, minutes and seconds).

Code: 8-4-2-1

Logic: Binary "1" = 0 (+0.5) volts
15 mA sink.
Binary "0" = +5 (±0.5) volts,
6 kΩ source.

Connector: Amphenol 57-40360.

**Option D11P:** Provides 20 lines of BCD outputs (hours, minutes and seconds).

Code: 8-4-2-1

Logic: Binary "1" = +5 (±0.5) volts,
6 kΩ source.
Binary "0" = 0 (+0.5) volts,
15 mA sink.

Connector: Amphenol 57-40360.

**Option E17:** Simultaneous Generate and Read.

# CHAPTER 2
# INSTALLATION

## 2.1 PRELIMINARY INSPECTION

As soon as the instrument is received, verify that it is intact and as ordered. If damage of any nature is found, refer to the warranty (behing title page) and to paragraph 2.4 for repackaging and shipping instructions.

## 2.2 ELECTRICAL INSPECTION

Before applying power or mounting the unit in a rack, remove the covers and ensure that all printed circuit cards are firmly mounted to the chassis and that no loose or broken wires or components are in evidence. Avoid changing the setting of any internal adjustment. Replace the covers and mount the unit as desired, taking care not to install it in close proximity to heat producing equipment.

## 2.3 INITIAL TURN-ON

The standard grounding type line cord, supplied with the equipment, should be connected first to unit's power connector and then to the primary power source. Push the POWER switch to the ON (button lighted) position and proceed with the operational checks of equipment functions. See Chapter 3 for operating procedures and Chapter 4 for recommended test equipment. If the equipment fails to perform correctly, contact the nearest Systron-Donner representative.

## 2.4 STORAGE AND RESHIPMENT

Environmental conditions during storage and shipment should be limited as follows:

Maximum Temperature: 185°F (85°C)

Minimum Temperature: -69°F (-55°C)

To protect your instrument during shipment or storage, use the best packaging methods available. Your Systron-Donner field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable packaging on short notice.

General packaging instructions:

(1) Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

(2) If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb./sq. inch bursting strength) or a wooden box to house the instrument.

(3) Use plenty of packaging material around all sides of the instrument and protect the frount panel with cardboard strips.

(4) Seal the package with strong tape

or metal bands. Mark with "Delicate Instrument".

(5) Refer to the warranty behind the title page of this manual and check with your Systron-Donner field office for shipping instructions. All correspondence should refer to the instrument by model number and full serial number.

## 2.5 POWER AND COOLING REQUIREMENTS

The Model 8350 can operate from 115 V or 230 V ±10%, 48 to 440 Hz approximately 30 watts. It is normally supplied for 115 volt operation.

To adapt the Model 8350 to 230 volt usage, remove the jumpers from pins 1 to 3 and 2 to 4 of the main power transformer and install a jumper between pins 2 and 3 of the transformer as shown on the power supply schematic Dwg. #21374-7-1 A. Refer to Figure 2.1.

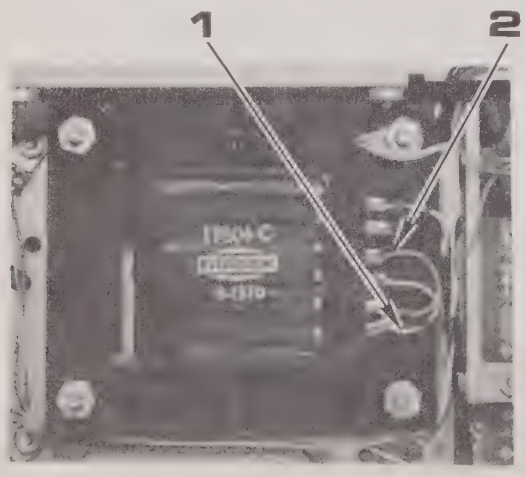


FIGURE 2.1
POWER TRANSFORMER WIRING

CAUTION

DISCONNECT ALL POWER FROM THE UNIT BEFORE CHANGING VOLTAGES.

There are no special cooling requirements when operating in the specified environmental conditions (0° to +50° C at up to 95% relative humidity).

## 2.6 INSTALLATION

The unit is normally supplied for bench top and tilt stand operation. If standard rack mounting is desired the following steps are necessary. (Refer to Figure 2.2).

(1) Remove the bottom cover to remove and retain the feet and tilt stand. Replace bottom cover.
(2) Remove the two handle holding screws from both sides at front of unit.
(3) Install rack mounting ears (supplied) on both sides at front of unit over the handles as shown.
(4) Remove one screw from both side panels at the rear of unit.
(5) Remove and retain two side trim panels. Side panels will slide out at back of the unit.
(6) Install the rear rack mounting adapter on both sides at rear of unit as shown. The rear rack mounting adapters fit in the groves provided for the side trim panels.
(7) Bolt the unit into the desired position.

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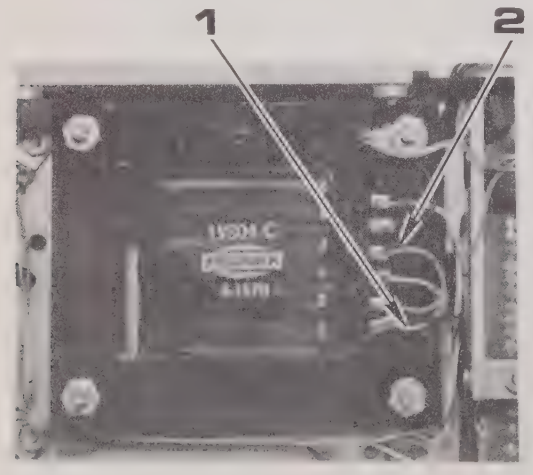


FIGURE 2.1
POWER TRANSFORMER WIRING

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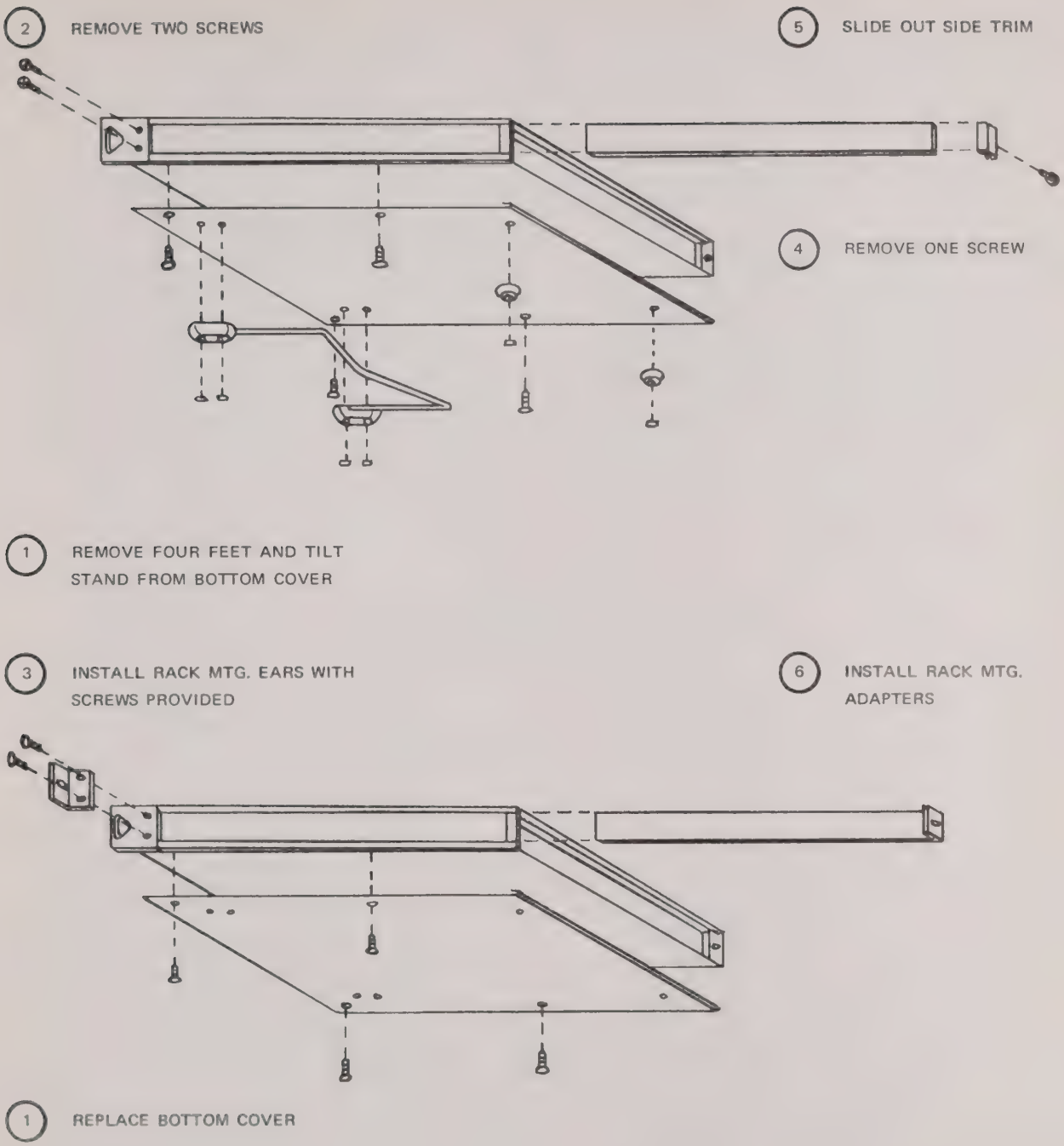



FIGURE 2.2
RACK MOUNTING

# CHAPTER 3
# OPERATION

## 3.1 GENERAL

The Model 8350 is ready to operate immediately after pushing on the power switch. Preliminary adjustments or calibration procedures are not normally required. It is advisable to read the following description, which describes the use of the controls and indicators, before using the unit.

## 3.2 CONTROLS, CONNECTORS AND INDICATORS

The operating controls, connectors and indicators of the Model 8350 Time Code Generator/Reader are listed in Table 3-1. Alignment controls are discussed in Chapter 4.

TABLE 3-1
CONTROLS, INDICATORS AND CONNECTORS

| Symbol | Name | Type | Function |
|---|---|---|---|
| (S1) | POWER | Pushbutton | Primary power switch. |
| (J1) | POWER IN | Standard, 3 prong | Primary power connector. |
| (F1,2) | FUSES | Fast Blow 1.0 A 115 V 0.5 A 230 V | AC power fuses. |
| (C1) | OSC. ADJ. | Variable Capacitor | Time Base frequency adjustment. |
| (J2) | CODE IN | BNC | Code Input Connector. |
| (J3) | CODE OUT | BNC | Code Output Connector. |
| (S2) | GEN | Pushbutton | Generate Mode Selector. |
| (S3) | READ | Pushbutton | Read (monitor) Mode Selector. |
| (S4) | HOLD | Pushbutton | Maintains accumulator contents at the initiate HOLD level. |
| (S5) | PRESET | Pushbutton | In conjunction with the HOLD switch sets accumulator to values displayed upon the preset thumbwheels. |
| (S6-9) | PRESET TIME | Thumbwheels | Determine initial start time. |
| (V1-6) | DISPLAY | Numerical Indicator Tubes | Provide visual display of accumulator contents in hours, minutes and seconds. |
| (DS1-4) | COLON | Miniatures Lamps | Separates the display's time increments. |
| (S11) | ERROR | Toggle Switch | Error Bypass On Off Switch. |
| (J4-7) | PULSE | BNC Connector | 1000, 100, 10 and 1 pps outputs. |

### 3.2.1 S1, POWER Pushbutton

This switch controls primary power to the unit. Application of ac line power to the unit with this switch in the "ON" position should not damage the instrument.

### 3.2.2 S2, GENerate Pushbutton

When this switch is pushed to ON, the Model 8350 acts as a Time Code Generator. The unit furnishes an output time code and the four pulse outputs. The display provides a visual indication of the output code.

### 3.2.3 S3, READ Pushbutton

This switch selects the Time Code Monitor mode of operation. The Model 8350 reads the modulated code input applied to CODE IN connector J2. The unit displays the accumulator contents and produces four pulse outputs which are synchronized to the incoming code.

### 3.2.4 S4, HOLD Pushbutton

S4, is used to command the Model 8350 to hold its accumulator contents indefinitely. The display remains stationary-set at the digital equivalent of the accumulator's contents at the time S4 was pushed and HOLD initiated. The accumulator is not updated again until the HOLD is released (GENerate pushbutton is despressed).

### 3.2.5 S5, PRESET Pushbutton

This control is an extension of the HOLD mode of operation. When the Model 8350 is in HOLD, momentarily depressing this switch effects the transfer, to the accumulator, of the PRESET start time (selected by thumbwheel PRESET TIME switches S6, S7, S8 and S9). The seconds digits are reset to zero.

### 3.2.6 S6, PRESET MINUTES Thumbwheel

Determines number of minutes to be preset into the accumulator in the PRESET mode.

### 3.2.7 S7, PRESET MINUTES X10 Thumbwheel

Determines number ot tens-of-minutes to be preset into the accumulator in the PRESET mode.

### 3.2.8 S8, PRESET HOURS Thumbwheel

Determines number of hours to preset into the accumulator in the PRESET mode.

### 3.2.9 S9, PRESET HOURS X10 Thumbwheel

Determines number of tens-of-hours to be preset into the accumulator in the PRESET mode.

### 3.2.10 S11, ERROR BYPASS Toggle Switch

Used in conjucntion with the READ mode of operation, this switch (in the ON position) allows the Model 8350 to read a time code, which is occasionally noisy or garbled, without losing synchronization.

# CHAPTER 3
# OPERATION

## 3.1 GENERAL

The Model 8350 is ready to operate immediately after pushing on the power switch. Preliminary adjustments or calibration procedures are not normally required. It is advisable to read the following description, which describes the use of the controls and indicators, before using the unit.

## 3.2 CONTROLS, CONNECTORS AND INDICATORS

The operating controls, connectors and indicators of the Model 8350 Time Code Generator/Reader are listed in Table 3-1. Alignment controls are discussed in Chapter 4.

TABLE 3-1
CONTROLS, INDICATORS AND CONNECTORS

| Symbol | Name | Type | Function |
|---|---|---|---|
| (S1) | POWER | Pushbutton | Primary power switch. |
| (J1) | POWER IN | Standard, 3 prong | Primary power connector. |
| (F1,2) | FUSES | Fast Blow 1.0 A 115 V 0.5 A 230 V | AC power fuses. |
| (C1) | OSC. ADJ. | Variable Capacitor | Time Base frequency adjustment. |
| (J2) | CODE IN | BNC | Code Input Connector. |
| (J3) | CODE OUT | BNC | Code Output Connector. |
| (S2) | GEN | Pushbutton | Generate Mode Selector. |
| (S3) | READ | Pushbutton | Read (monitor) Mode Selector. |
| (S4) | HOLD | Pushbutton | Maintains accumulator contents at the initiate HOLD level. |
| (S5) | PRESET | Pushbutton | In conjunction with the HOLD switch sets accumulator to values displayed upon the preset thumbwheels. |
| (S6-9) | PRESET TIME | Thumbwheels | Determine initial start time. |
| (V1-6) | DISPLAY | Numerical Indicator Tubes | Provide visual display of accumulator contents in hours, minutes and seconds. |
| (DS1-4) | COLON | Miniatures Lamps | Separates the display's time increments. |
| (S11) | ERROR | Toggle Switch | Error Bypass On Off Switch. |
| (J4-7) | PULSE | BNC Connector | 1000, 100, 10 and 1 pps outputs. |

### 3.2.1 S1, POWER Pushbutton

This switch controls primary power to the unit. Application of ac line power to the unit with this switch in the "ON" position should not damage the instrument.

### 3.2.2 S2, GENerate Pushbutton

When this switch is pushed to ON, the Model 8350 acts as a Time Code Generator. The unit furnishes an output time code and the four pulse outputs. The display provides a visual indication of the output code.

### 3.2.3 S3, READ Pushbutton

This switch selects the Time Code Monitor mode of operation. The Model 8350 reads the modulated code input applied to CODE IN connector J2. The unit displays the accumulator contents and produces four pulse outputs which are synchronized to the incoming code.

### 3.2.4 S4, HOLD Pushbutton

S4, is used to command the Model 8350 to hold its accumulator contents indefinitely. The display remains stationary-set at the digital equivalent of the accumulator's contents at the time S4 was pushed and HOLD initiated. The accumulator is not updated again until the HOLD is released (GENerate pushbutton is despressed).

### 3.2.5 S5, PRESET Pushbutton

This control is an extension of the HOLD mode of operation. When the Model 8350 is in HOLD, momentarily depressing this switch effects the transfer, to the accumulator, of the PRESET start time (selected by thumbwheel PRESET TIME switches S6, S7, S8 and S9). The seconds digits are reset to zero.

### 3.2.6 S6, PRESET MINUTES Thumbwheel

Determines number of minutes to be preset into the accumulator in the PRESET mode.

### 3.2.7 S7, PRESET MINUTES X10 Thumbwheel

Determines number ot tens-of-minutes to be preset into the accumulator in the PRESET mode.

### 3.2.8 S8, PRESET HOURS Thumbwheel

Determines number of hours to preset into the accumulator in the PRESET mode.

### 3.2.9 S9, PRESET HOURS X10 Thumbwheel

Determines number of tens-of-hours to be preset into the accumulator in the PRESET mode.

### 3.2.10 S11, ERROR BYPASS Toggle Switch

Used in conjucntion with the READ mode of operation, this switch (in the ON position) allows the Model 8350 to read a time code, which is occasionally noisy or garbled, without losing synchronization.

### 3.3 TIME CODE GENERATOR OPERATION

To operate the Model 8350 as a time code generator, the following steps are necessary:

(1) Push S1, POWER Switch, to ON (button lighted).

(2) Push S4, HOLD switch, to ON (button lighted).

(3) Adjust PRESET TIME Thumbwheels, S6 through S9, for desired preset (initial start) time.

(4) Push S5, PRESET switch. The accumulator is updated to the preselected start time. The unit is now generating a repetitive time code equal to the static numerical display.

(5) Push S2, GEN (generate) switch to ON (button lighted).

The Model 8350 should now be generating a time code (modified IRIG B) the first frame of which represents the preselected start time. The code is updated, thereafter, once each second. The generated code is made available at connector J3, CODE OUT, on the rear panel.

### 3.4 TIME CODE READER OPERATION

To operate the Model 8350 as a time code reader the following steps are necessary.

(1) Push S1, POWER switch, to ON (button lighted).

(2) Connect a time code (either IRIG B or modified IRIG B) or (IRIG E or XR 3 if so equipped) input to connector J2, CODE IN, on the rear panel.

(3) Place ERROR BYPASS switch S11, in the desired position.

(4) Push S3, READ switch, to ON (button lighted).

The Model 8350 should now be monitoring the input code.* The readout will display the code's time-of-day information and will change at the on-time point in each code frame. The Model 8350 will read code, if desired, at a much faster rate than the rate at which the time code was recorded.

### 3.5 USE OF PULSE OUTPUTS

The pulse outputs (1 k pps, 100 pps, 10 pps and 1 pps). made available on the rear panel (connectors J7, J6, J5 and J4 respectively, are generated in the time base dividers with the pulses positive transitions "on-time". Therefore, the pulses can be used as interpolation marks and perform timed logic control functions.

*The AGC circuitry may take up to 20 seconds to reach its specified operating level after initial power turn-on.

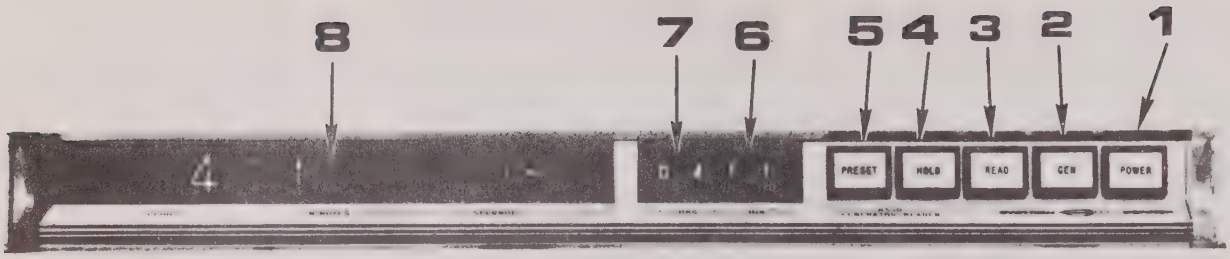



FIGURE 3.1
FRONT PANEL CONTROLS AND INDICATORS

(1) POWER PUSHBUTTON — This switch controls main power to the unit.

(2) GEN PUSHBUTTON — This MODE switch when depressed commands the unit to function as a Time Code Generator.

(3) READ PUSHBUTTON — This Mode switch when depressed commands the Time Code Monitor function.

(4) HOLD PUSHBUTTON — This Mode switch when depressed commands the Hold function. This causes the accumulator content to be stopped and continously displayed until the HOLD is released (GEN pushbutton depressed).

(5) PRESET PUSHBUTTON — This switch when depressed extends the HOLD mode operation (HOLD mode activated) by transferrring the PRESET start time (selected by HRS, MIN thumbwheel switches) into the accumulator.

(6) MIN THUMBWHEELS — These switches selects the number of minutes and tens of minutes to be set into the accumulator when presetting start time.

(7) HRS THUMBWHEELS — These switches select the number of hours and tens of hours to be set into the accumulator when presetting start time.

(8) DISPLAY COUNTERS — The six digit DISPLAY COUNTER will continuously display the internally generated time or the time decoded from an incoming time code.

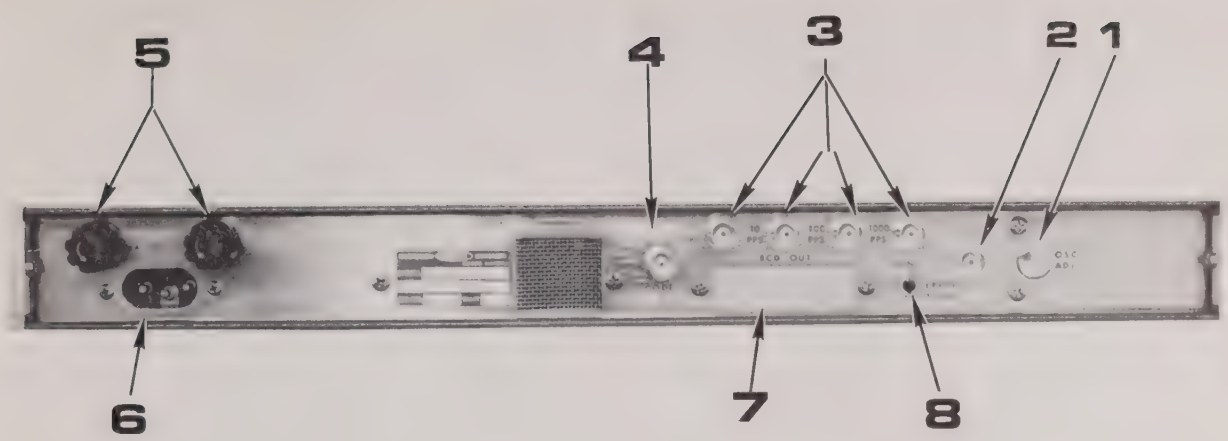



FIGURE 3.2
REAR PANEL CONTROLS AND CONNECTORS

| | | |
|---|---|---|
| (1) | OSC ADJ | This variable capacitor provides time base frequency calibration and adjustment from the rear panel. |
| (2) | CODE OUT | Output jack for the internally generated code when in the GENerate function. |
| (3) | PULSE RATE OUTPUTS | These pulse rate output jacks provide individual precisely controlled pulse trains (synchronized with the generated or incoming time code) of 1000 pps, 100 pps, 10 pps and 1 pps for external timing pulses or to provide time interpolation down to 1 millisecond. |
| (4) | CODE IN | Inputs jack to receive the time code to be read when in READ function. |
| (5) | FUSES | Primary (1.0 A Fast Blow 115 V or 0.5 A Fast Blow 230 V) power fuses. |
| (6) | RECEPTICLE | For use with the power cord supplied. |
| (7) | BCD OUT | Optional; provides 20 lines of BCD outputs (hours, minutes and seconds) to be used for remote displays or other applications. |
| (8) | ERROR BYPASS | This switch (in the ON position) when in the READ function allows reading of up to three consecutive noisy time frames without losing synchronization. |

# CHAPTER 4
# MAINTENANCE AND CALIBRATION

## 4.1 FACTORY SERVICE

When the instrument requires service, the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns when necessary. Address all inquiries on operation or applications to your nearest sales representative, or to:

Sales Manager
Data Products Division
Systron-Donner Corporation
888 Galindo Street
Concord, California 94520

Specify both model and complete serial number in all correspondence.

## 4.2 ROUTINE MAINTENANCE

A regular program for routine maintenance and inspection every twelve months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

(1) Disconnect ac power and remove the top and bottom covers.

(2) Make a thorough visual inspection of all wiring and cables.

(3) Check for physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage. When a printed circuit board contains integrated circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

(4) Check all rear panel switches and connectors for loose or broken terminals, loose or sticking shafts, etc.

(5) If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and a low pressure stream of air to remove the foreign material.

CAUTION

DO NOT CLEAN PC BOARDS OR SMALL INTERNAL COMPONENTS WITH A STIFF BRUSH OF SOLVENTS, SINCE DAMAGE TO THE CIRCUITS MAY RESULT. A HIGH-POWERED VACUUM CLEANER SHOULD NOT BE USED ON SMALL INTERNAL COMPONENTS.

(6) Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints and other foreign material.

(7) Clean the polarizing filter window only, using a soft cloth and warm, soapy water: ABRASIVES OR SOLVENTS WILL DAMAGE THE FILTER. If desired, the filter may be removed for cleaning (remove trim and slide the filter out the end). The surfaces of the indicator tubes may be cleaned with a damp cloth at this time.

(8) Perform the Operational Test and Calibration Procedure (Paragraph 4.6).

If performanace does not match or exceed the specifications listed in Chapter I of this manual, corrective maintenance is in order.

## 4.3 PRINTED-CIRCUIT BOARD REPAIR

To remove a part on a printed circuit board, cut the leads of the part near the lead holes. Using a low power (50 watts or less) soldering iron, apply heat sparingly to each cut lead. As soon as the solder melts, slip the lead from the hole and clean the hole with a toothpick. Clean the board surfaces with isopropyl alcohol. Form the tinned leads of the replacement part and insert in cleaned holes, trimming the leads to extend 1/16 inch beyond the back surface of the board. Only 63/37 solder with a maximum diameter of 1/16 inch should be used. Solder the leads to the boards and use a hemostat, long-nosed pliers, or other heat sink on the leads of all semi-conductor devices and quarter-watt resistors. Allow the soldered junction to cool before removing the heat sink.

Integrated circuit packages are best removed by carefully melting the solder around each pin and sudsing it out with a vacuum device from the backside of the board. After the solder has been removed from all pins, carefully loosen each pin with needle nose pliers, then lift out the package.

**WARNING**

**DANGEROUS HIGH VOLTAGES ARE PRESENT ON THE POWER SUPPLY AND DISPLAY CIRCUITS OF THIS EQUIPMENT. EXERCISE CAUTION AT ALL TIMES WHEN THE PROTECTIVE COVERS HAVE BEEN REMOVED.**

## 4.4 TEST EQUIPMENT

The following test equipment or its equivalent is recommended for use in servicing the Model 8350 Time Code Generator/Reader:

| MODEL | MANUFACTURER | DESCRIPTION |
|---|---|---|
| 531A | Tektronix, Inc. | Oscilloscope, 15 MHz bandwith, triggered sweeps from 0.1 microseconds/cm to 1 second/cm. |
| CA | Tektronix, Inc. | Dual trace calibrated pre-amp for 531A oscilloscope, 0.05 volts/cm to 20 volts/cm. |
| P6000 | Tektronix, Inc. | Probe: 10 to 1 attenuation ratio, 12 pfd capacitance. |
| 260 | Simpson | VOM: 20,000 ohm/volts dc sensitivity plus or minus 3% accuracy. |

In addition to test equipment listed above, a suitable source of input signals with known characteristics may be required. This may be another time code generator or a pre-recorded tape and its associated tape play-back equipment. Also, if the oscillator is to be adjusted, a 1 kHz or higher precision frequency source (5 parts in $10^7$ short term stability) is required.

## 4.5 CALIBRATION CONTROLS

With the top chassis cover removed, the

the factory set calibration controls are readily accessible. In general, these controls should need adjustment only if components are replaced or the controls are inadvertently disturbed. The modulated output code amplitude and modulation ratio controls, HOWEVER, should be adjusted per environmental requirements. The calibration controls, listed in Table 4-1 and shown in Figure 4.1, are in their correct calibration sequence.

### 4.5.1 Calibration Control and Board Locations

"A" items are located on the Power Supply Board.
"B" items are located on the Input-Output Board.
"C" item, located on the rear panel, is labeled OSC. ADJ.

Access to items A and B, require removal of the top cover. The Logic Board is located beneath the bottom cover. Both the Display-Readout and Oscillator-Decade Boards are mounted perpendicular to the top and bottom chassis covers.

## 4.6 CALIBRATION PROCEDURES

The following procedures are used to calibrate the Model 8350. When shipped from the factory, the unit is completely aligned and no further adjustment should be necessary, the modulated code output amplitude and modulation ratio controls excepted (See paragraph 4.5). Perform the steps in their listed order since earlier steps may effect later ones.

### 4.6.1 Power Supply Adjustment and Inspection

(1) Connect the Model 8350, via a Variac (set to 115 volts), to 115 V ac or to 230 V ac on unit having the 230 volt power supply.
(2) Push POWER switch to ON.
(3) Place GEN pushbutton to the ON (button lighted) position.
(4) Connect the voltmeter to the +15 volt test point on the power supply board.
(5) Adjust R4 for +15 ±0.5 volts. Connect an oscilloscope to the +15 volt test point and check ripple (100 mV peak-to-peak or less).
(6) In the same manner as Step 5, monitor the 5 volt test point and adjust R14 for +5 ±0.15 volts (ripple: 100 mV peak-to-peak or less).
(7) As above, monitor the -15 volt test point and adjust R8 for -15 ±0.5 volts (ripple: 100 mV peak-to-peak or less).
(8) Monitor the +225 volt line for +225 ±25 volts with ripple less than 2 V peak-to-peak.
(9) Measure each voltage above with the Variac set first at 105 V ac and then at 130 V ac. The voltages (+225 volts

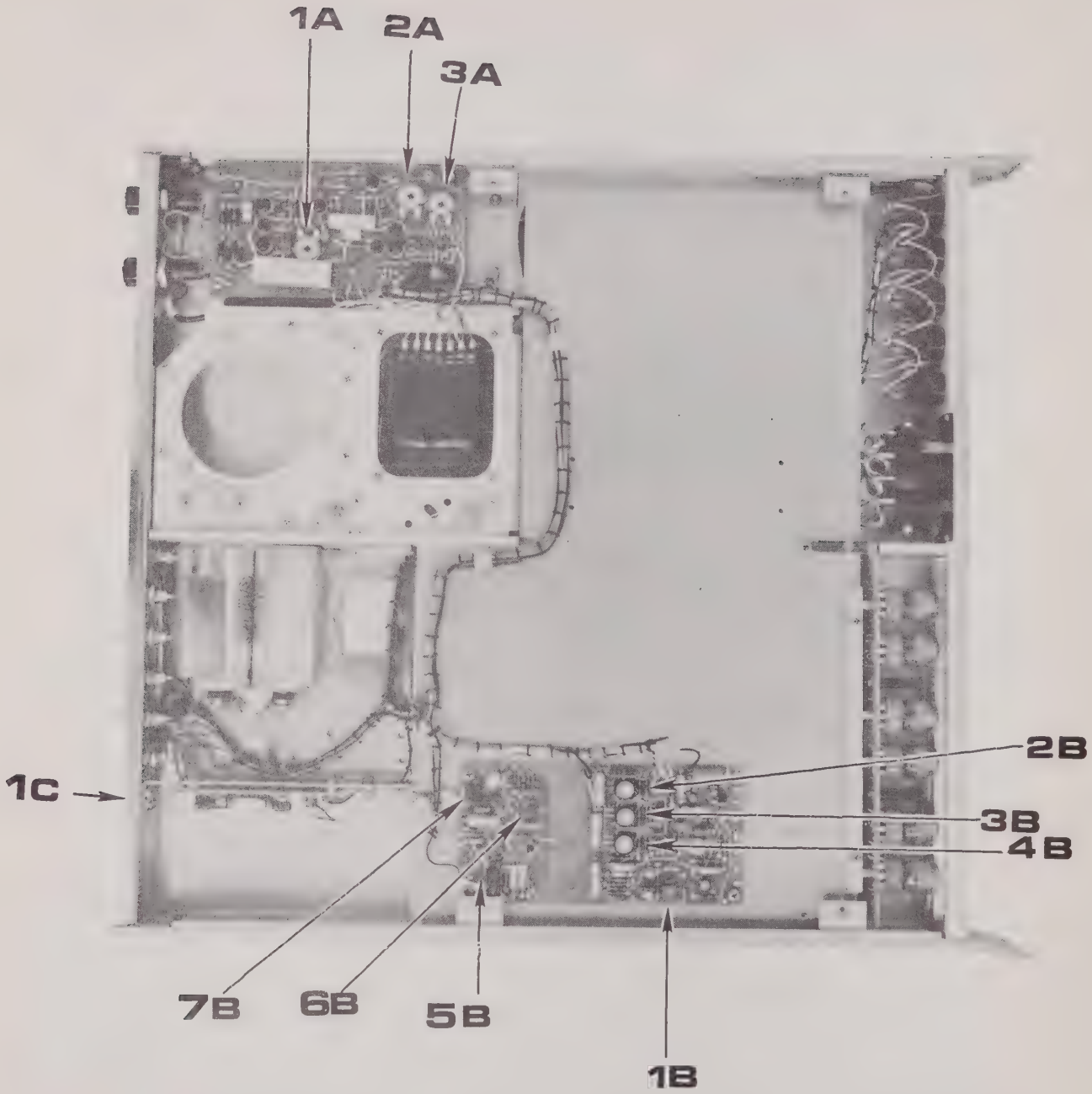



FIGURE 4.1
CALIBRATION CONTROLS LOCATION

excepted) should stay within the above specifications. On units having the 230 volt power, measure each voltage above with the Variac set first at 210 V ac and then at 250 V ac. The voltages (+225 volts excepted) should stay within the above specifications.

### 4.6.3 Adjust Level of Modulated Code

With the oscilloscope, monitor the time code output at J3, on rear panel. Adjust the Large Cycle amplitude to the desired level (Factory adjusted to 3 volts peak-to-peak) with R17 on the Input-Output Board.

TABLE 4-1

CALIBRATION CONTROLS

| CONTROL | LOCATION | FUNCTION |
|---|---|---|
| R7 | 1A | Adjusts output of +15 volt regulator. |
| R15 | 2A | Adjusts output of +5 volt regulator. |
| R23 | 3A | Adjusts output of -15 volt regulator. |
| C1 | 1C | Time Base Frequency adjustment. |
| R17 | 7B | Modulated Code output amplitude adjustment. |
| R13 | 6B | Modulation Ratio Adjustment. |
| R5 | 5B | Modulated code phase adjustment. |
| R37 | 1B | AGC level adjustment. |
| R44 | 3B | Adjusts Lower Large Cycle Trigger Level. |
| R48 | 4B | Adjusts Upper Large Cycle Trigger Level. |
| R40 | 2B | Adjusts each Cycle Trigger Level. |

### 4.6.2 Time Base Frequency Adjustment

With the Model 8350 in GEN (Generate), synchronize the oscilloscope with the 100 pps output at J7 on the rear panel. Observe the frequency standard's output on the scope. Adjust C1 (OSC. ADJ.), located on the rear panel, for a stable trace.

### 4.6.4 Adjust Modulation Ratio of Modulated Code

With the oscilloscope, monitor the modulated code output at J3, on Model 8350 rear panel. Adjust the Small Cycle amplitude to the desired level (Factory adjusted to 1 volt peak-to-peak) with R13

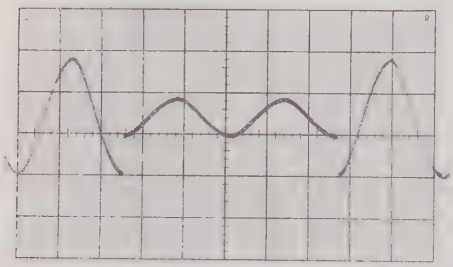
on the input output board.

### 4.6.5 Phase Adjustment of Modulated Code

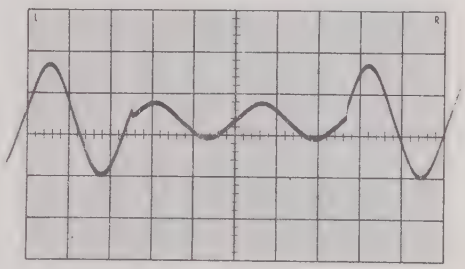
With the oscilloscope, monitor the modulated code output at J3, on Model 8350 rear panel. Adjust R5, on the Input-Output Board, until smooth transitions from "Large to Small" and "Small to Large" Cycles are observed. (Figure 4.2).

### 4.6.6 AGC Adjustment

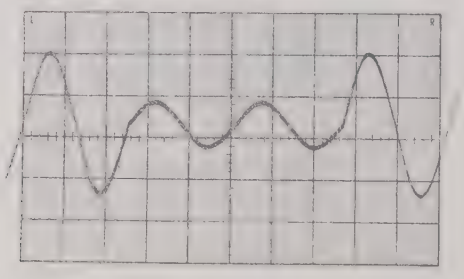
Apply a suitable time code to CODE IN connector J2, (the output time code at connector J3 will do nicely) located on the Model 8350 rear panel. On the Input-Output Board, with the oscilloscope, Monitor the positive end of capacitor C17. Adjust AGC potentiometer R37 (Input-Output Board) for 2 volts peak-to-peak Large Cycles.



INCORRECT ADJUSTMENT
R5 FULLY CLOCKWISE



INCORRECT ADJUSTMENT
R5 FULLY COUNTER CLOCKWISE



R5 CORRECTLY ADJUSTED

FIGURE 4.2
MODULATED CODE PHASE
ADJUSTMENT

NOTE:

The delayed AGC requires approximately 8 seconds to recover.

### 4.6.7 Set Lower Large Cycle

Monitor Input-Output Board pin 3 with the oscilloscope. Adjust R44 (Input-Output Board) until the rectangular signals, analagous to the time code Large Cycles, *marginally* appear on the oscilloscope (adjust for the point at which these rectangular signals just begin to appear on the oscilloscope). (Figure 4.3)

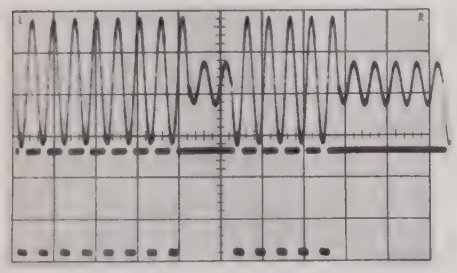


FIGURE 4.3
R44 LOWER LARGE
CYCLE TRIGGER
CORRECTLY ADJUSTED

### 4.6.8 Set Upper Large Cycle

Monitor Input-Output Board pin 4 with the oscilloscope. Adjust R48 (Input-Output Board) until the rectangular signals, analagous to the time code Large Cycles, *marginally* appear on the oscilloscope (adjust for the point at which these rectangular signals just begin to appear on the oscilloscope). (Figure 4.4).

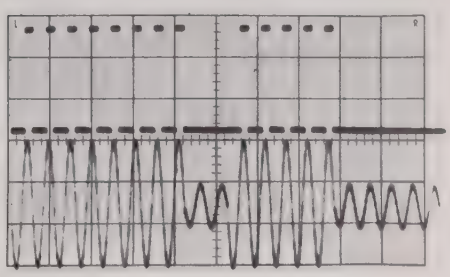


FIGURE 4.4
R48 UPPER LARGE
CYCLE TRIGGER
CORRECTLY ADJUSTED

### 4.6.9 Adjust Each Cycle Detector

With the oscilloscope, monitor the positive end of capacitor C17 (Input-Output Board). Adjust AGC potentiometer R37 (In-Out Board) for 0.5 volt peak-to-peak Small Cycles.

NOTE

The delayed AGC requires approximately 8 seconds to recover.

With the oscilloscope, monitor Input-Output Board pin 2. Adjust R40 until the rectangular pulses, analagous to the time code carrier frequency, appear on the oscilloscope.

NOTE

A range of adjustment should exist which will produce the proper indication. R40 should be placed in the center of this range. (Figure 4.5).

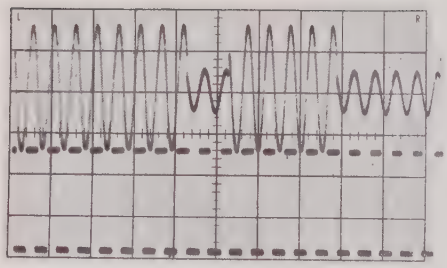


FIGURE 4.5
R40 EACH CYCLE TRIGGER
CORRECTLY ADJUSTED

### 4.6.10 Final AGC Adjustment

With the oscilloscope, monitor the positive end of the capacitor C17 (Input-Output Board), adjust the Large Cycles amplitude to 3 volts peak-to-peak.

NOTE

The delayed AGC requires approximately 8 seconds to recover.

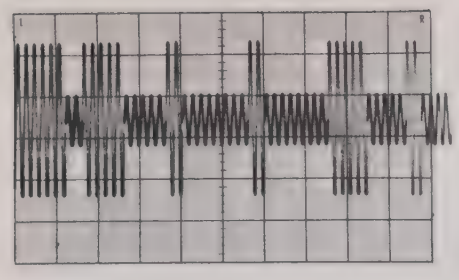
### 4.6.11 READ (Monitor) Test

Remove the oscilloscope. Depress the READ pushbutton. The Model 8350 (time code still applied to CODE IN connector J2) should be operational.

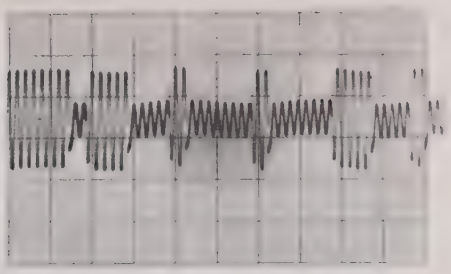
## 4.7 READ MODE CODE INPUT COMPARISONS

Figure 4.6 illustrates some typical tape transport code inputs when in the READ function.

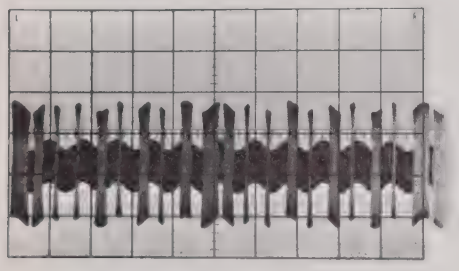
The Model 8350 can be expected to read inputs with considerable deviation from the ideal code input (Figure 4.6.1). If it fails to read a code, the transport input should be observed and considered as a possible cause of the failure.



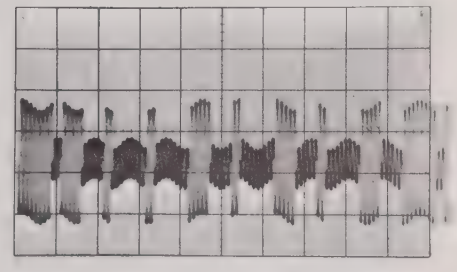
4.6.1
IDEAL IRIG B TIME CODE SHOWS
FRAME MARKER AND NINE SECONDS



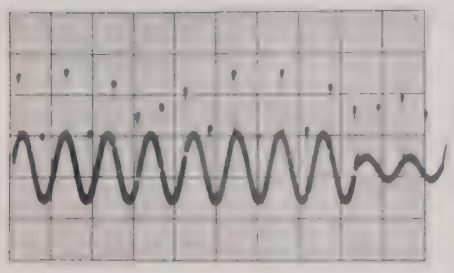
4.6.2
SAME AS 4.6.1 WITH UNDESIRABLE
PHASE SHIFTS



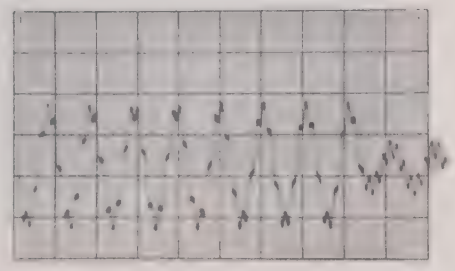
4.6.3
60 Hz RIPPLE RIDING IRIG B CODE



4.6.4
120 Hz RIPPLE RIDING IRIG B CODE



4.6.5
HIGH FREQUENCY NOISE PULSES
ON CODE



4.6.6
SPURIOUS NOISE RIDING
CODE

FIGURE 4.6
READ MODE CODE INPUT COMPARISONS

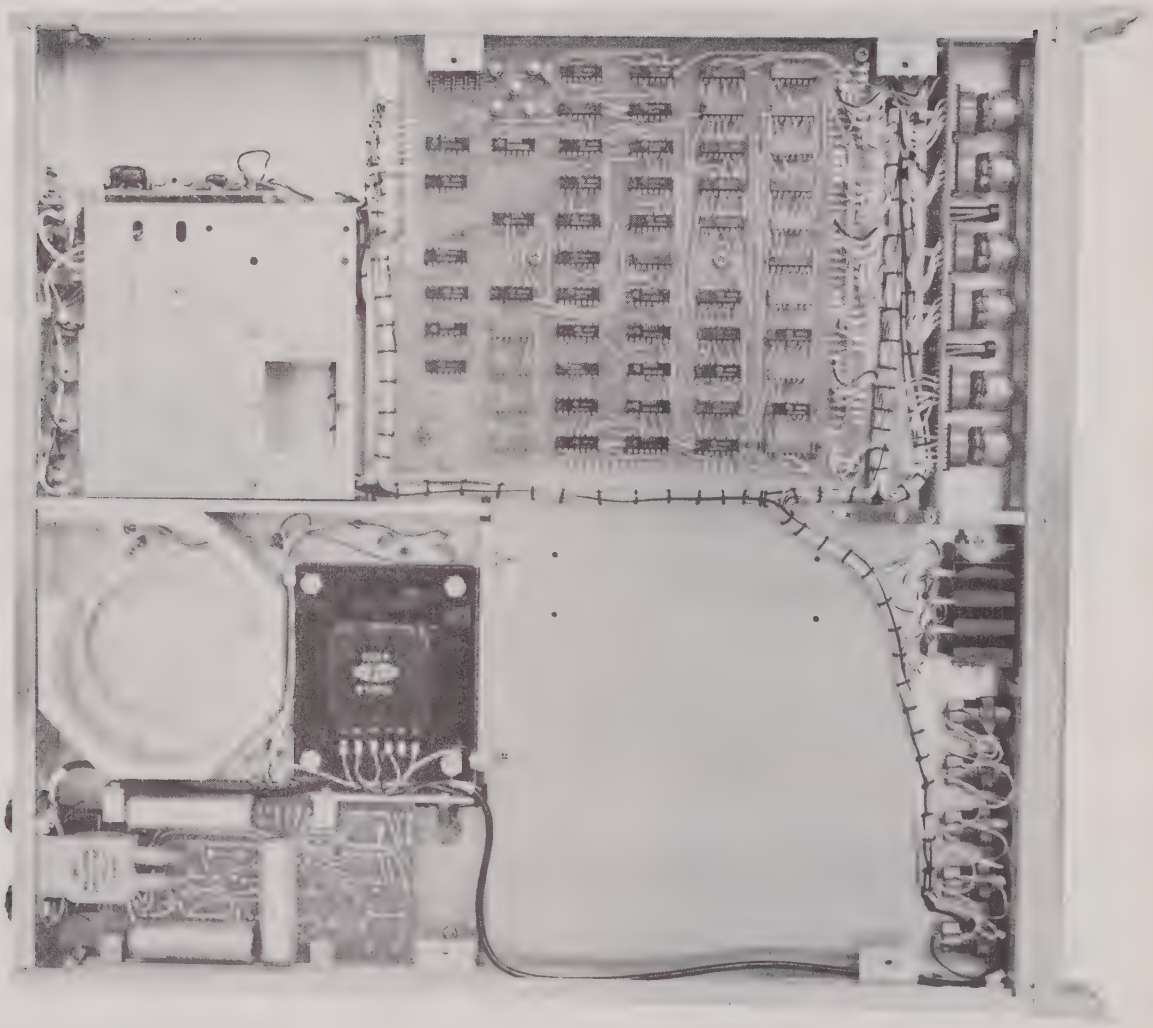


FIGURE 4.7
MODEL 8350 IRIG B
BOTTOM VIEW COVER REMOVED

# CHAPTER 5
# FUNCTIONAL DESCRIPTION

## 5.1 GENERAL

The Model 8350 Wiring Block Diagram, Dwg. #31000-7-1 depicts the complete instrument and is used for this Functional Description. Additional reference drawings are as called out on the Wiring Block Diagram.

The time codes of the standard Model 8350 is of the IRIG B format. Other codes can be supplied as options.

## 5.2 FUNCTIONAL

The Model 8350 uses a single logic board to perform the majority of the functions necessary for operation of the instrument. For example, this board contains divider decades, scan gates, error bypass circuitry and code generation and detection circuitry.

An Input-Output Board provides signal conditioning for the received code and produces the modulated code.

The Oscillator Decade Board provides the master timing signals used in the instrument. Its output is a 1 kHz signal

A BCD Output Board (Optional) provides buffered logic level (+5 volts NOM from a 6 kΩ source) outputs which are available on a rear panel connector.

Complete descriptions of all standard circuit cards and assemblies are contained in Chapter 6.

## 5.3 IRIG FORMAT "B"

1. TIME: Universal Time (UT-2)

2. TIME FRAME: 1.0 Second

3. CODE DIGIT WEIGHTING OPTIONS: *BCD, SB or both:*

    a. Binary Coded Decimal time-of-year *Code Word* – 30 binary digits
        (1) Seconds, minutes, hours, and days
        (2) Recycles each 24 hours

4. *Code Word* structure:

    a. *BCD:* Word begins at *Index Count 1.* Binary coded Elements occur between *Position Identifier Elements* (7 for seconds, 7 for minutes; 6 for hours; 8 and 2 for days) until the *Code Word* is complete. An *Index Marker* occurs between decimal digits in each group to provide separation for visual resolution.
    b. *SB:* Word begins at *Index Count 80.* Five decimal digits (17 binary coded elements) occur with a *Position Identifier* between the 9th and 10th binary coded elements.

5. Least significant digit occurs first.

6. ELEMENT RATES AVAILABLE:

    a. 100 per second (basic Element rate)
    b. 10 per second
    c. 1 second

7. ELEMENT IDENTIFICATION:

    a. "On time" reference point for all Elements is the leading edge.
    b. Index Marker . . . . . 2 milliseconds
    (Binary Zero or uncoded Element)
    c. Code Digit . . . . . 5 milliseconds
    (Binary One)
    d. Position Identifier . . . . . 8 milliseconds
    (Refers to the leading edge of the succeeding Element)
    e. Reference Marker – 1 per second. . . . . Two consecutive *Position Identifiers*
    (The "on time" point, to which the *Code Word* refers, is the leading edge of the second *Position Identifier*.)

8. RESOLUTION: 10 milliseconds (unmodulated)
    1 milliseconds (modulated)

9. CARRIER FREQUENCY: 1 kc when modulated

# CHAPTER 5
# FUNCTIONAL DESCRIPTION

## 5.1 GENERAL

The Model 8350 Wiring Block Diagram, Dwg. #31000-7-1 depicts the complete instrument and is used for this Functional Description. Additional reference drawings are as called out on the Wiring Block Diagram.

The time codes of the standard Model 8350 is of the IRIG B format. Other codes can be supplied as options.

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The Model 8350 uses a single logic board to perform the majority of the functions necessary for operation of the instrument. For example, this board contains divider decades, scan gates, error bypass circuitry and code generation and detection circuitry.

An Input-Output Board provides signal conditioning for the received code and produces the modulated code.

The Oscillator Decade Board provides the master timing signals used in the instrument. Its output is a 1 kHz signal

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3. CODE DIGIT WEIGHTING OPTIONS: *BCD, SB or both:*
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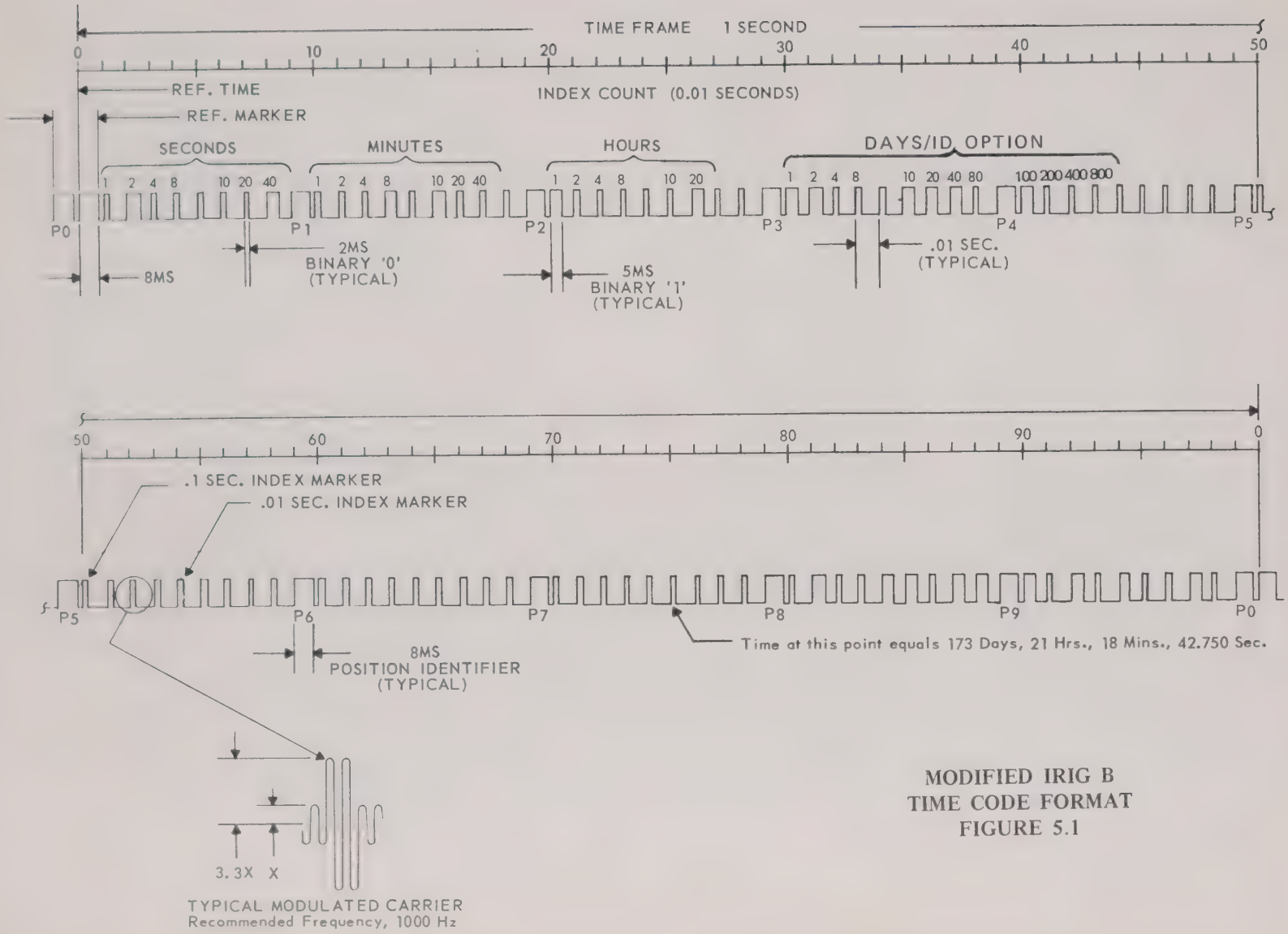
        (1) Seconds, minutes, hours, and days
        (2) Recycles each 24 hours
4. *Code Word* structure:
    a. *BCD:* Word begins at *Index Count 1.* Binary coded Elements occur between *Position Identifier Elements* (7 for seconds, 7 for minutes; 6 for hours; 8 and 2 for days) until the *Code Word* is complete. An *Index Marker* occurs between decimal digits in each group to provide separation for visual resolution.
    b. *SB:* Word begins at *Index Count 80.* Five decimal digits (17 binary coded elements) occur with a *Position Identifier* between the 9th and 10th binary coded elements.
5. Least significant digit occurs first.
6. ELEMENT RATES AVAILABLE:
    a. 100 per second (basic Element rate)
    b. 10 per second
    c. 1 second
7. ELEMENT IDENTIFICATION:
    a. "On time" reference point for all Elements is the leading edge.
    b. Index Marker . . . . . 2 milliseconds
    (Binary Zero or uncoded Element)
    c. Code Digit . . . . . 5 milliseconds
    (Binary One)
    d. Position Identifier . . . . . 8 milliseconds
    (Refers to the leading edge of the succeeding Element)
    e. Reference Marker – 1 per second. . . . . Two consecutive *Position Identifiers*
    (The "on time" point, to which the *Code Word* refers, is the leading edge of the second *Position Identifier*.)
8. RESOLUTION: 10 milliseconds (unmodulated)
    1 milliseconds (modulated)
9. CARRIER FREQUENCY: 1 kc when modulated




MODIFIED IRIG B
TIME CODE FORMAT
FIGURE 5.1

## 5.4 IRIG FORMAT "E"

1. TIME: Universal Time UTC

2. TIME FRAME: 10 Seconds

3. CODE DIGIT WEIGHTING OPTIONS: *BCD' SB or both:*

   a. Binary Coded Decimal time-of-year *Code Word* – 26 binary digits
      (1) Tens of seconds, minutes, hours and days
      (2) Recycles yearly

   b. Straight binary time-of-day *Code Word* – 17 binary digits
      (1) Seconds only (every 10 seconds)
      (2) Recycles each 24 hours

4. *Code Word* structure

   a. *BCD:* Word begins at *Index Count* 6. Binary coded elements occur between *Position Identifier Elements* (3 for seconds; 7 for minutes; 6 for hours; 8 and 2 for days) until the *Code Word* is complete. An *Index Marker* occurs between decimal digits in each group to provide separation for visual resolution.

   b. *SB:* Word begins at *Index Count* 80. Five decimal digits (17 binary coded elements) occur with a *Position Identifier* between the 9th and 10th binary coded elements.

5. Least significant digit occurs first.

6. ELEMENT RATES AVAILABLE:

   a. 10 per second (basic element rate).
   b. 1 per second
   c. 1 per 10 seconds

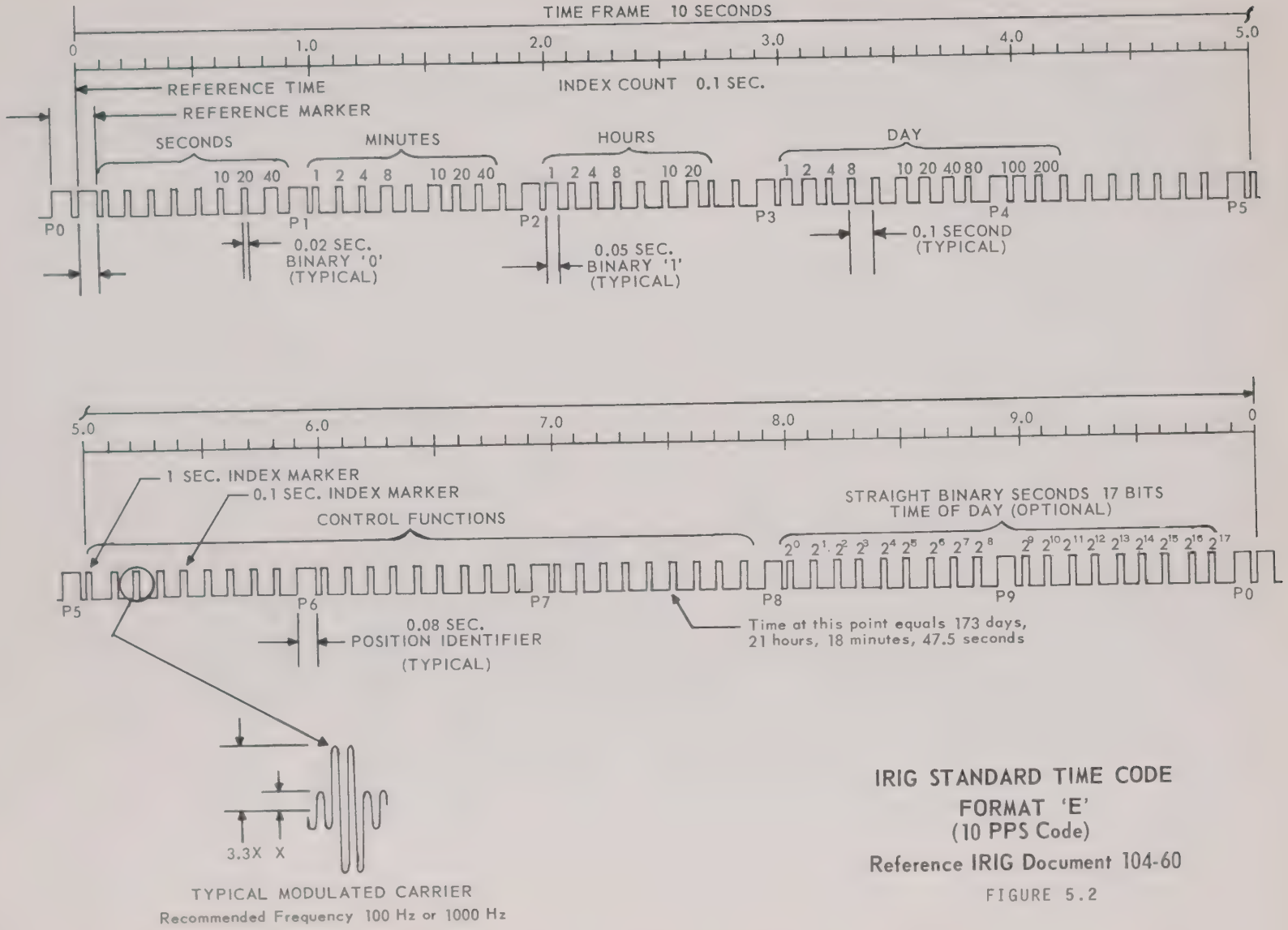
7. ELEMENT IDENTIFICATION:

   a. "On time" reference point for all elements is the leading edge.
   b. Index Marker — 20 milliseconds
      (Binary "O" or uncoded element
   c. Code Digit — 50 milliseconds
      (Binary "1")
   d. Position Identifier – 1 per second — 80 milliseconds
      (Refers to the leading edge of the succeeding element)
   e. Reference Marker – 1 per 10 seconds — Two consecutive *Position Identifiers*

   (The "on time" point, to which the *Code Word* refers, is the leading edge of the second *Position Identifier.)*

8. RESOLUTION: 100 milliseconds (unmodulated)
   10 milliseconds (modulated 100 cycles)
   1 millisecond (modulated 1000 cycles)

9. CARRIER FREQUENCY: 100 or 1000 cycles when modulated




TYPICAL MODULATED CARRIER
Recommended Frequency 100 Hz or 1000 Hz

## IRIG STANDARD TIME CODE
## FORMAT 'E'
## (10 PPS Code)

Reference IRIG Document 104-60

FIGURE 5.2

## 5.5 XR 3 FORMAT

1. **TIME:** Universal Time (UT-2)

2. **TIME FRAME:** 1.0 Second

3. **CODE DIGIT WEIGHTING:** *BCD*

   a. Binary Coded Decimal time-of-day *Code Word*——20 binary digits
      (1) Hours, minutes, seconds
      (2) Recycles each 24 hours

4. **CODE WORD STRUCTURE BCD:**

   Word begins following Reference Marker. First 6 Bits are hours, next 7 are minutes and final 7 are seconds.

5. **MOST SIGNIFICANT DIGIT OCCURS FIRST**

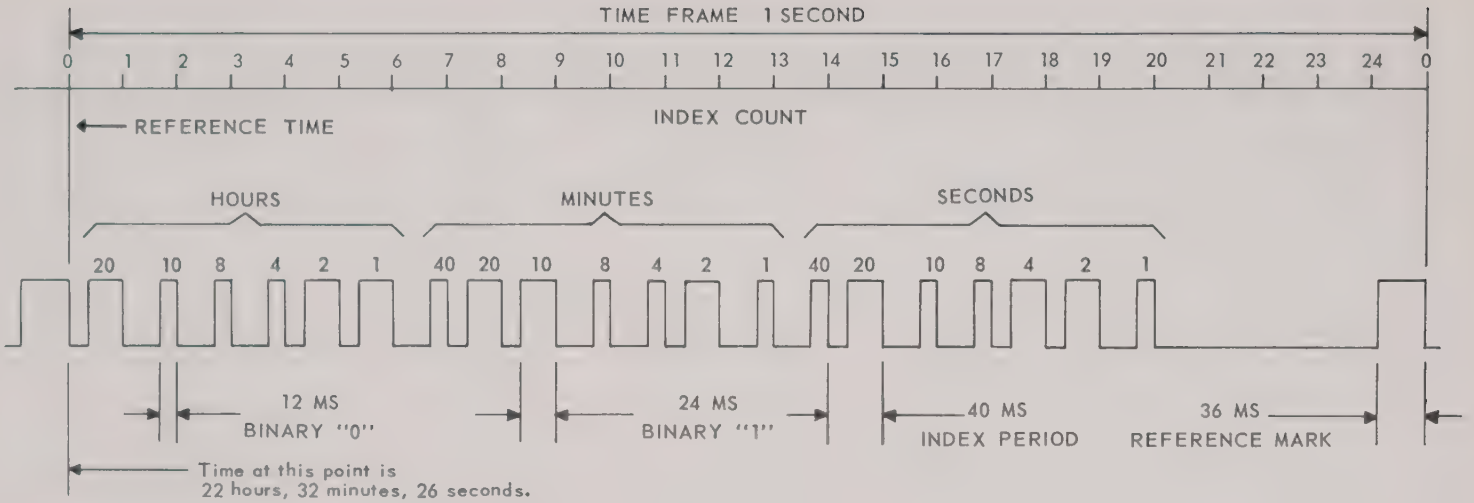
6. **BIT RATE 25 pps**

7. **ELEMENT IDENTIFICATION:**

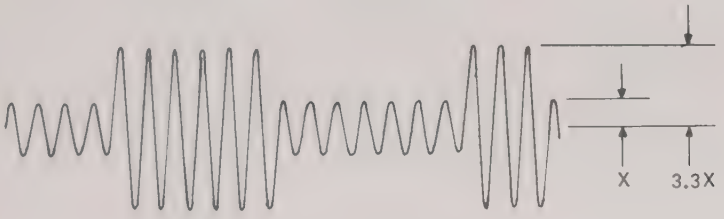
   a. "On Time" reference point for all elements is the trailing edge.
   b. Code Digit (Binary Zero) . . . . . .12 milliseconds
   c. Code Digit (Binary One). . . . . .24 milliseconds
   d. Reference Marker——1 per second . . . . .36 milliseconds
   (The "on time" point, to which the *Code Word* refers, is the trailing edge of the Reference Marker.

8. **RESOLUTION:** 4 milliseconds (modulated) (250 Hz)
   1 millisecond (modulated) (1 kHz)

9. **CARRIER FREQUENCY:** 250 Hz or 1 kHz when modulated




NOTE: Trailing edge of each mark is on time.




TYPICAL MODULATED CARRIER

Normal Carrier Frequency – 250 Hz
Other Frequencies in use – 1 KHz
6.25 KHz
100 KHz

**XR-3 TIME CODE**
**(25 PPS Code)**

**Also known as**
**803 CODE**

FIGURE 5.3

# CHAPTER 6
# CIRCUIT DESCRIPTIONS

## 6.1 POWER SUPPLY (Dwg #21374-7-1)

This power supply provides both regulated and unregulated voltages from either a 115 V or 230 V, 50 to 60 Hz power source. Primary power arrives at primary windings 1-2-3-4 of power transformer T1 from the ac line cord through a line filter, fuses F1 and F2, POWER switch S1, and LINE SELECTOR switch S6. The power transformer provides three separate secondary windings from which the following voltages are obtained: +225 V dc, +15 V dc, -15 V dc, +5 V dc.

### +225 V Supply (unregulated)

The +225 V dc supply voltage is produced in the following manner: approximately 185 V rms from the T1 secondary windings is full wave rectified by the bridge consisting of CR1, CR2, CR3, and CR4 producing +225 V dc filtered by C6 and R23.

### +15 V Supply (regulated)

The +15 V dc regulated voltage supply is based on 1/2 of the 38 V rms center tapped secondary winding 9-6-10 and full wave rectifiers CR5 and CR8. The +22 V dc is filtered by C10 and fed to the collector of series pass transistor Q8 and to pins 7 and 8 of the I.C. regulator U1. U1 drives the base of Q8 and regulates the +15 V dc supply. The level adjust is R4.

### -15 V Supply (regulated)

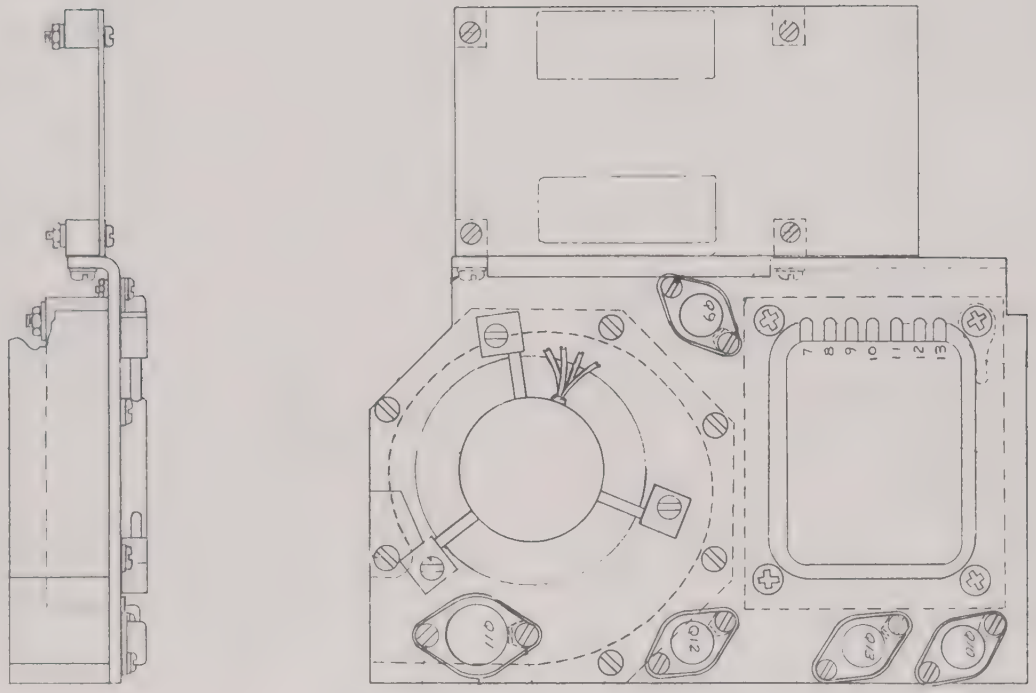
The -15 V dc regulated supply is produced by CR6 and CR7 and the 9-6-10 secondary windings of T1. The -22 V dc is filtered by C11 and fed to the collector of series pass transistor Q10 which is driven by transistor Q2 and diode Q1. I.C. U2 regulates the -15 V dc with R8 acting as a level adjust.

### +5 V Supply (regulated)

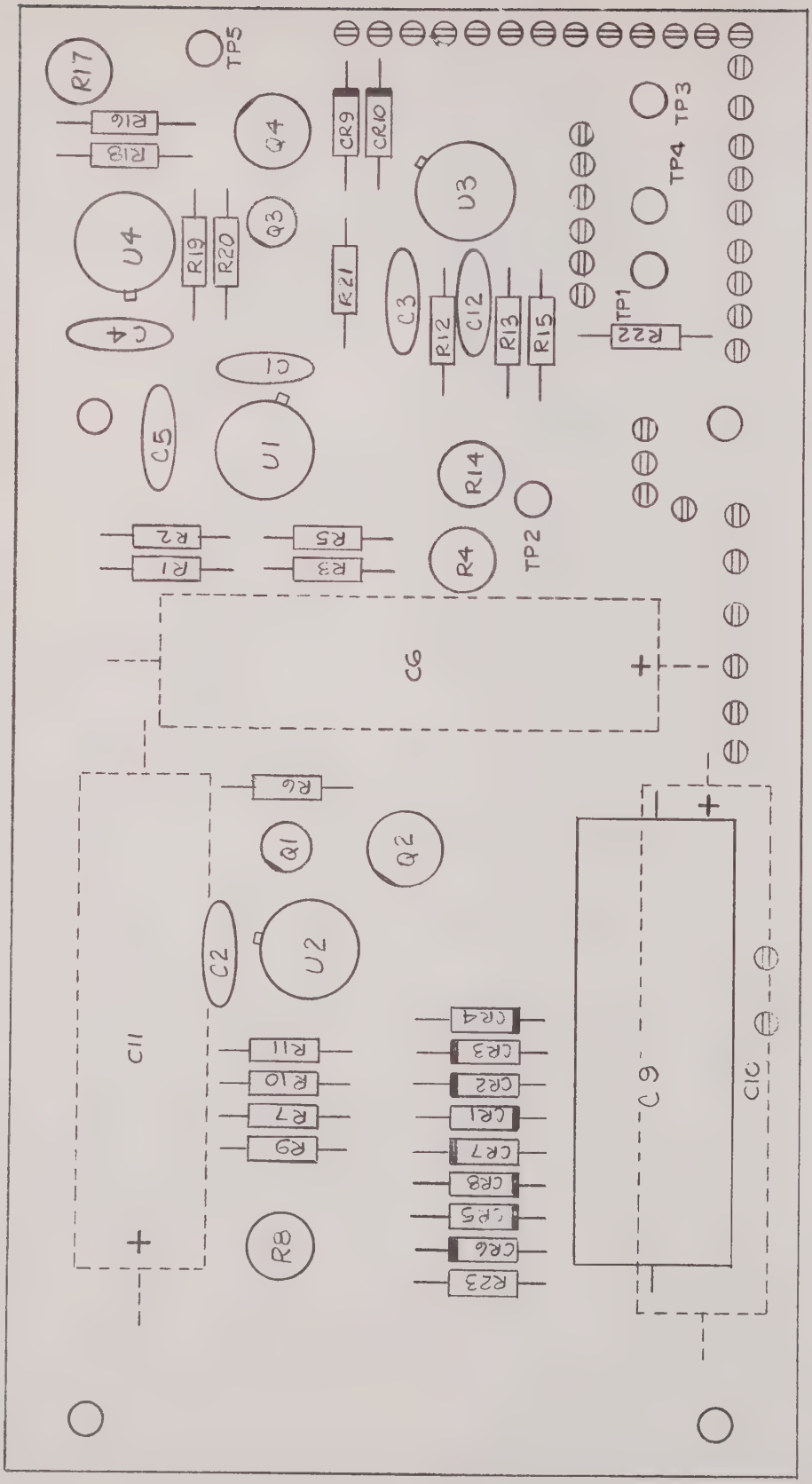
Similar to the +15 V dc supply, the +5 V dc regulated supply is derived from T1 secondary 11-12-13, rectifiers CR19 and CR20, and filter C7. The +9 V is ten regulated by I.C. U3 and referenced to the +15 V supply. U3 powers Q12 which drives series pass transistor Q13. R14 adjusts the level.

PARTS LIST

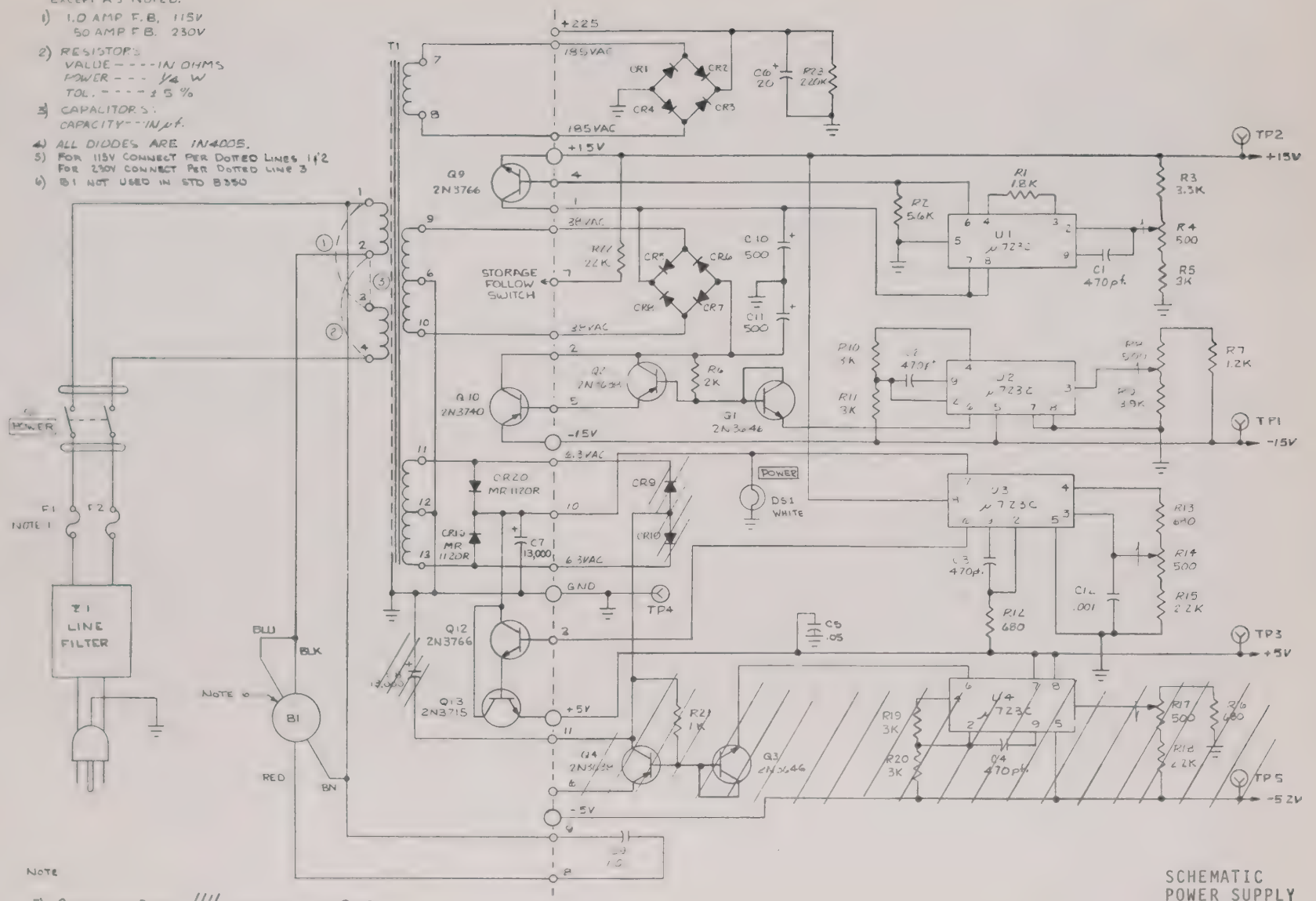
| Ref. | Description | Part No. |
|---|---|---|
| | Power Supply P.C. Assembly | D39464C |
| | Power Supply Schematic | C21374-7-1 |
| C1-4 | Capacitor, 470 pF, 300 V | C0542 |
| C5 | Capacitor, 05 µF, 12 V | C0672 |
| C6 | Capacitor, 20 µF, 350 V | C1094 |
| C9 | Capacitor, 1 µF, 400 V | C0724 |
| C10,11 | Capacitor, 500 µF, 30 V | C1134 |
| C12 | Capacitor, .001 µF, 1000 V | C0235 |
| CR1-10 | Diode, IN4005 | CR0284 |
| Q1-4 | Transistor, 2N3638 | Q0181 |
| R1 | Resistor, 1.8 k, 1/4 W, 5% | R0959 |
| R2 | Resistor, 5.6 k, 1/4 W, 5% | R0821 |
| R3 | Resistor, 3.3 k, 1/4 W, 5% | R0742 |
| R4,8,14,17 | Resistor, 500 Ω, Pot. | R2375 |
| R5,10,11, 19,20 | Resistor, 3 k, 1/4 W, 5% | R0711 |
| R6 | Resistor, 2 k, 1/4 W, 5% | R0734 |
| R7 | Resistor, 1.2 k, 1/4 W, 5% | R0809 |
| R9 | Resistor, 3.9 k, 1/4 W, 5% | R0939 |
| R12,13,16 | Resistor, 680 Ω, 1/4 W, 5% | R1234 |
| R15,18 | Resistor, 2.2 k, 1/4 W, 5% | R0749 |
| R21 | Resistor, 1 k, 1/4 W, 5% | R0765 |
| R22 | Resistor, 22 k, 1/4 W, 5% | R0768 |
| R23 | Resistor, 220 k, 1/4 W, 5% | R0967 |
| U1-4 | Integrated Circuit, 723C | 25756 |




ASSEMBLY
POWER SUPPLY
19734 B




POWER SUPPLY
P.C. ASSEMBLY
39464 C




SCHEMATIC
POWER SUPPLY
MODEL 8350
21374-7-1 B

## 6.2 TIME-OF-DAY ACCUMULATOR (Dwg. #21494-7-1)

### General

This portion of the Model 8350 contains three integrated circuit divide by ten counters, two divide by six counters and two flip-flops. The counters accumulate time-of-day in hours, minutes and seconds, may be preset, and the hours counters are recycled at 23:59:59.

### Counting Circuit

Integrated circuit divider A1, A3, A5, A7 and A9 and dual flip-flop A21 successively divide the 1 pps input signal to accumulate the time-of-day. Dual flip-flop A21 is used for tens of hours. Gates A11 are used to strobe the preset or scan in information to the tens of hours counter. For example if pin 42 is high (a ONE to be preset) A11-3 will be low, A11-6 will be high causing the clear input to set $\overline{Q}$ (the output) high, for a ONE. The integrated circuit divider preset is accomplished via diodes on the data input lines.

### Recycle Circuit

To reset the hours counters following 23:59:59, gate A17-6 goes low at a count of 24. This sets flip-flop A19-6/A19-3 low causing a low input to the preset in inputs of A21-5 and A21-9 and the reset input of A9. The $\overline{Q}$ outputs of A21-5 and A21-9 and all outputs of A9 go low under this condition. The inverted 100 pps signal from the Z counter will reset the flip-flop 8 ms later removing the recycle signal. This 8 ms interval insures that sufficient time is available for reset.

During the preset, double inverter A27-10/A27-8 holds the flip-flop high, insuring that A9, A21-5 and A21-9 are not being reset while presetting them.

## 6.3 CONTROL CIRCUITS (Dwg. #21494-7-1)

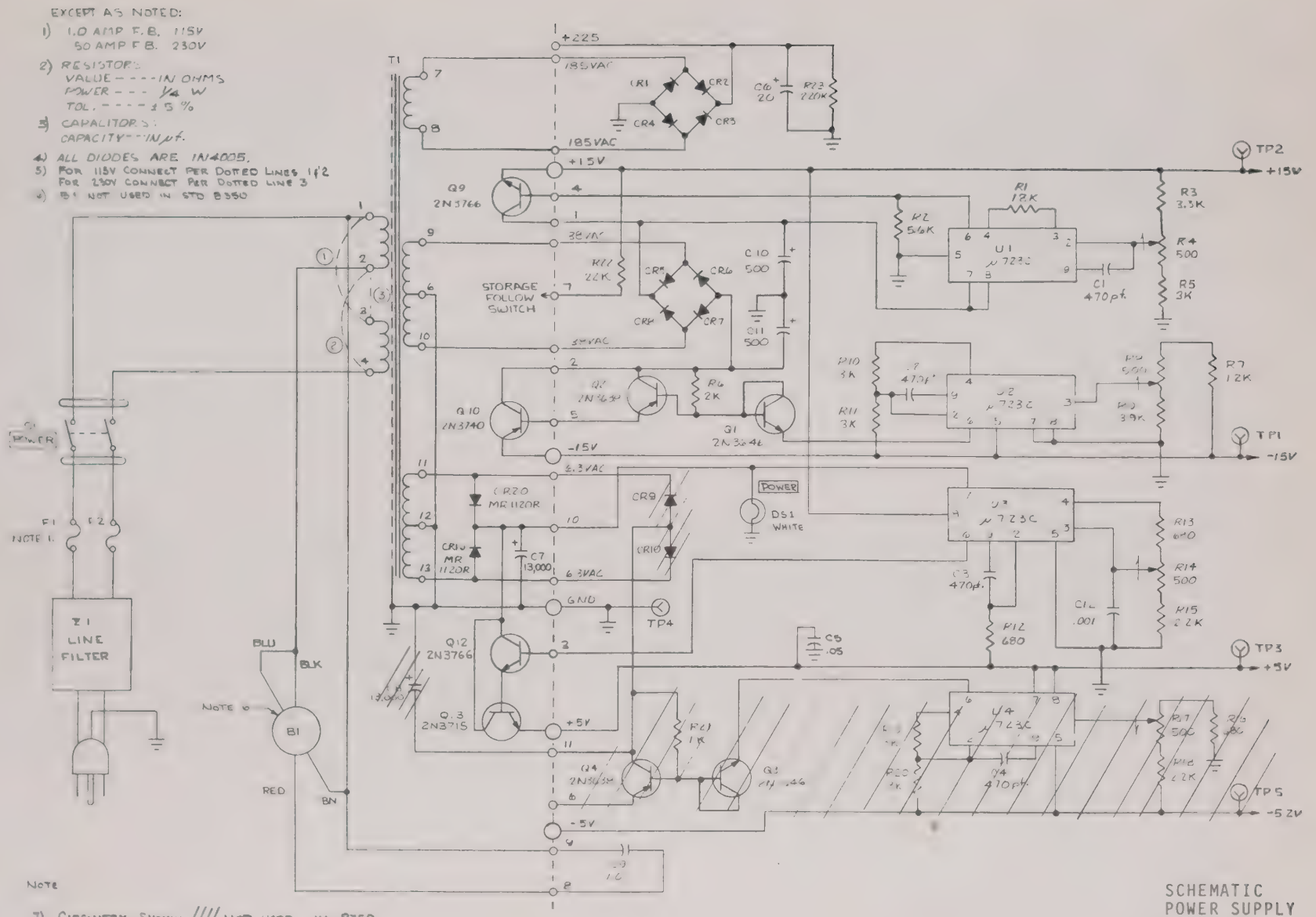
### General

Front panel controls for selecting READ, GENerate, HOLD and PRESET are momentary contact pushbuttons. Four thumbwheel switches are used to preset the minutes and hours digits (seconds are always preset to ZERO).

### READ, GENerate, HOLD circuits.

Three flip-flops are used to store commands generated by the front panel pushbuttons. For example the GENerate button causes flip-flop A56-8/A50-6 to set the output high. If either the HOLD or READ buttons are pushed, A56-8/A50-6 will reset and flip-flop associated with the button pushed will set.

Transistor Q1 lights the lamps in both the HOLD and PRESET buttons when in HOLD Mode. The PRESET button is illuminated to indicate that preset may be initiated. Q2 lights the GENerate button lamps and


EXCEPT AS NOTED:
1) 1.0 AMP F.B. 115V
.50 AMP F.B. 230V
2) RESISTORS:
VALUE - - - - IN OHMS
POWER - - - 1/4 W
TOL. - - - - ± 5 %
3) CAPACITORS:
CAPACITY - - - IN μf.
4) ALL DIODES ARE 1N4005.
5) FOR 115V CONNECT PER DOTTED LINES 1 & 2
FOR 230V CONNECT PER DOTTED LINE 3
6) B1 NOT USED IN STD 8350
T1
+22.5
18.5VAC
CR1
CR2
CR3
CR4
C6 20
R23 220K
TP2
+15V
Q9 2N3766
38VAC
R11 22K
STORAGE FOLLOW SWITCH
CR5
CR6
CR7
CR8
C10 500
C11 500
55VAC
Q10 2N3740
Q2 2N3638
R6 2K
Q1 2N3646
-15V
TP1
-15V
6.3VAC
CR20 MR1120R
CR9
CR10
CR19 MR1120R
C7 13,000
6.3VAC
GND
TP4
POWER
DS1 WHITE
R1 12K
R2 5.6K
U1 μA723C
C1 470pf
R3 3.3K
R4 500
R5 3K
R10 3K
C2 470pf
U2 μA723C
R9 500
R8 3.9K
R7 12K
R11 3K
U3 μA723C
R13 680
R14 500
R15 2.2K
C3 470pf
C4 .001
R12 680
C5 .05
TP3
+5V
Q12 2N3766
Q3 2N3715
+5V
R21 1K
Q4 2N3638
Q5 2N3646
U4 μA723C
R17 500
R16 2.2K
R20 2K
C9 470pf
TP5
-5.2V
-5V
C8 .1
C
POWER
F1
F2
NOTE 1
Z1 LINE FILTER
BLU
BLK
NOTE 6
B1
RED
BN
NOTE
7) CIRCUITRY SHOWN //// NOT USED IN 8350
SCHEMATIC
POWER SUPPLY
MODEL 8350
21374-7-1 B

## 6.2 TIME-OF-DAY ACCUMULATOR (Dwg. #21494-7-1)

### General

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### Counting Circuit

Integrated circuit divider A1, A3, A5, A7 and A9 and dual flip-flop A21 successively divide the 1 pps input signal to accumulate the time-of-day. Dual flip-flop A21 is used for tens of hours. Gates A11 are used to strobe the preset or scan in information to the tens of hours counter. For example if pin 42 is high (a ONE to be preset) A11-3 will be low, A11-6 will be high causing the clear input to set $\overline{Q}$ (the output) high, for a ONE. The integrated circuit divider preset is accomplished via diodes on the data input lines.

### Recycle Circuit

To reset the hours counters following 23:59:59, gate A17-6 goes low at a count of 24. This sets flip-flop A19-6/A19-3 low causing a low input to the preset in inputs of A21-5 and A21-9 and the reset input of A9. The $\overline{Q}$ outputs of A21-5 and A21-9 and all outputs of A9 go low under this condition. The inverted 100 pps signal from the Z counter will reset the flip-flop 8 ms later removing the recycle signal. This 8 ms interval insures that sufficient time is available for reset.

During the preset, double inverter A27-10/A27-8 holds the flip-flop high, insuring that A9, A21-5 and A21-9 are not being reset while presetting them.

## 6.3 CONTROL CIRCUITS (Dwg. #21494-7-1)

### General

Front panel controls for selecting READ, GENerate, HOLD and PRESET are momentary contact pushbuttons. Four thumbwheel switches are used to preset the minutes and hours digits (seconds are always preset to ZERO).

### READ, GENerate, HOLD circuits.

Three flip-flops are used to store commands generated by the front panel pushbuttons. For example the GENerate button causes flip-flop A56-8/A50-6 to set the output high. If either the HOLD or READ buttons are pushed, A56-8/A50-6 will reset and flip-flop associated with the button pushed will set.

Transistor Q1 lights the lamps in both the HOLD and PRESET buttons when in HOLD Mode. The PRESET button is illuminated to indicate that preset may be initiated. Q2 lights the GENerate button lamps and

Q3 the READ button lamp. Q5 is required to sink the current from the twenty gates and one flip-flop to which it is connected. It provides a logical ZERO when in other than Read Mode. Q4 provides a logical ZERO when in Hold to enable the Preset thumbwheels and inhibit the 1 pps (via gate A32-8).

PRESET CIRCUIT

The Outputs from the four thumbwheel switches are diode connected to the data inputs of the minutes and hours decade counters (one switch for each counter). When in the Hold Mode, pushing the PRESET button will cause the preset numbers to load into the counters by pulling the appropriate strobe lines down via a set of diodes. The seconds digits are preset at ZERO by grounding the reset line on the associated dividers with the PRESET button.

## 6.4 BIT DETECTOR (Dwg. #21494-7-1)

### General

The bit detector is used to produce serial ONES from the received code and to detect both the single MARKS and the double MARK which occurs at the start of the time frame. Refer to the timing diagram, Figure 6.2 for this section.

### Bit Counter

Integrated circuit A47 is a divide by 10 counter whose input is the gated ULC signal. Gate A55-3 allows the ULC signal to input A47 only when in the read mode. Also, counter A47 is held reset to 0,0,0,0 when in other than Read. Flip-flop A49-5 is used to preset A47 to 1,0,0,0 once each 10 ms, the first time a LLC pulse occurs. A51-8 will hold the preset on A49-5 low keeping Q high and not presetting A47 when not in Read. A52-10 will prevent the 100 pps from the Z counter from inputting the clock line of A49-5 when not in Read.

Referring to Figure 6.2, note that one ULC has passed before a LLC has preset A47. Thus the reason for starting A47 with one count. The outputs of A47 are gated by A51-6 to produce a signal at the count of seven. This indicates the presence of a MARK. A41-6/A1-3 will produce an output from the time A51-6 goes low until the 100 pps ("8" bit) from the Z counter goes low. A 41-8/A43-12 will go up at the first MARK received and will be reset when either A43-6 or A43-8 go low. A43-6 goes low to indicate a ONE in the received code, A43-8 goes low with a ZERO. Note that capacitor C1 is used to slow down the rise of A41-8/A43-12.

Flip-flop A31-5 is used to provide a signal when two consecutive MARKS have been received (start of frame). This signal is used by the error bypass circuit.

The output from flip-flop A41-8/A43-12 drives the D input of A31-5. The clock of A31-5 is driven (via an inverter) from the output of A51-6. The first received MARK sets A41-8/A43-12 and simultaneously clocks A31-5. The capacitor, C1 on the D input of A31-5 slows the rise sufficiently to prevent A31-5 from changing state. If, however, another MARK is received prior to any ONES or ZEROS (this is the case at the start of the frame double MARK) A31-5 will receive another clock pulse. Since the D line has been up for some time, the flip-flop will change state. The output of A41-11 provides a clear signal for A31-5 every 10 ms and thus, A31-5 puts out a short pulse each time a double MARK is received.

The output of A43-6 is the received $\overline{\text{SERIAL ONES}}$. This is used to scan in data to the accumulators when enabled by the error bypass circuit.

Gates A55-6 and A55-8 are used to select the EC signal as an input to the counter chain when in read mode and the internal 1 k pps when not in Read. Gates A55-11 and A50-11 provide buffered outputs of the EC/1 k pps (positive transistion on time).

## 6.5 COUNTER (Dwg. #21494-7-1)

### General

Three integrated circuit counters successively divide the 1 k pps/EC signal by 10 to yield a 1 pps signal.

### Counters

A46, the Z counter, has an output of 100 pps. This counter will be reset to ZERO each time A49-5 output goes low. This synchronizes the start of count. The data preset is used to parallel load a count of seven each time A51-6 goes low. This insures that the Z counter and the bit counter (A47) are synchronized after receipt of a MARK. Counters A45 and A44 are reset by A31-5 once each frame. This reset insures synchronization of the X and Y counters. Both A45 and A44 should be at ZERO at the reset time.

### Outputs

Gate A48-3 provides a buffered 100 pps from the Z counter. A48-11 provides the 10 pps signal and A32-11 the 1 pps signal. All three outputs are positive transistion on time.

Gates A32-8 and A32-6 provide the 1 pps update for the accumulators. A32-8 allows an output at all times except when in Hold.

## 6.6 BCD TO DECIMAL DECODERS (Dwg. #21494-7-1)

### General

Two identical decoding networks are used to provide the X and Y times for scan gates. Each decoder combines the BCD outputs of a decade counter to produce decimal outputs.

For example decimal seven requires that the 1, 2, and 4 bit lines be up. The 2 and 4 bits are AND gated (and inverted in the process) the 1 bit is simply inverted. A NOR gate is used which requires both inputs low for high output.

## 6.7 SCAN IN CIRCUIT (Dwg. #21494-7-1)

### General

The scan in circuits is composed of three sections, the strobe gates, the scan in gates and the four bit shift register. The scan in circuit is used to load the accumulator with data from the received code.

### Shift Register

Four flip-flop are connected to form a non-recirculating shift register. Refer to Figure 6.1 for the timing of the various signals.

The serial ONES line from the received code in connected to the "D" input of the first flip-flop, A30-5. The Q output feeds the 8 bit inputs of the three divide by 10 counters via inverting gates. In this way when a serial ONE is present, A30-5 will have a low output at Q which will be inverted before it is loaded into a divider. Since the $\overline{Q}$ output of A30-5 feeds A30-9, it is necessary to use the $\overline{Q}$ output from A30-9, A29-5 and A29-9 to maintain proper polarity.

The operation of the shift register is as follows:

The clock lines of all four flip-flops are energized once each 10 ms by the shift line. This causes the Q output to assume the same state as the "D" input. The shift register runs continuously and its outputs are strobed into the appropriate counter at the correct time.

### Strobe Gates

The strobe circuits for loading the three divide by ten stages are identical, only the times are different. Refer to the IRIG B time code format. At an index count of five (Y0, X5), the register will contain (from left to right) the 8 bit, 4 bit, 2 bit, and 1 bit for unit seconds. Therefore, gate A12-8, which strobes the unit seconds decade has as its inputs the X5 time, Y0 time and the scan in enable from the error bypass.

Similarly, at an index count of 14 the register will contain unit minutes information and gate A12-12 will strobe the unit minutes decade at X4, Y1 time. The unit hours will be strobed at X4, Y2 time (index count of 24).

The tens of seconds counter is strobed at X0, Y1 time. At this time the first flip-flop in the register does not con-

tain any code information. Note that A3, the tens of seconds decade, has no connection to A30-5 output.

The tens of minutes counter is strobed at X8, Y1 time. In this case the last flip-flop does not contain code information and there is no connection between it and A7.

Tens of hours is strobed at S8, Y2 time. Neither the first nor the last flip-flop of the shift register contain code information and, therefore, are not used by the tens of hours flip-flops.

### Scan In Gates

Each input to a counter has a control gate associated with it. This gate is enabled only in the Read Mode, thus preventing scan in at other times. Diodes are used to allow preset, where used.

## 6.8 ERROR BYPASS (Dwg. #21494-7-1)

### General

The error bypass circuit permits inhibiting scan in of information unless three senssecutive bad frames are received. With good data being received, the accumulators are updated by the EC signal.

### Error Detector

Gates A40-3, A40-6, and A40-8 form an exclusive OR gate. The $\overline{\text{SERIAL ONES}}$ from the scan out of the accumulators is compared to the $\overline{\text{SERIAL ONES}}$ from the received code. As long as both are the same, the input to A40-11 will be high. Should a difference exist, the input to A40-11 will go low. Gate A39-6 is necessary for two reasons. First, since the Model 8350 does not generate DAYS data, any DAYS information in the received code would appear to be an error. The input on pin 4 of A39-6 (from A39-8) will enable the gate only during the first 300 ms of the frame (when seconds, minutes and hours data is present). Second, duty cycle of the received $\overline{\text{SERIAL ONES}}$ and the internal $\overline{\text{SERIAL ONES}}$ is not the same. The input on pin 3 of A39-6 enables the gate during a time when both are present. Thus, only actual errors will cause A39-6 to go low.

### Error Flip-Flop

Flip-flops A37-5 and A37-9 will accumulate up to a count of three and are used to store the number consecutive bad frames. The input of A37-5 is clocked once each frame by the output of A31-5. Flip-flop A31-9 will be set by A31-5 once per frame. If no errors are present, A31-9 will remain set, enabling gate A38-6. Under this condition A37-5 and A37-9 will receive a clear signal with each clock signal, keeping both their outputs low. When an error is present, A31-9 will be reset prior to the clock pulse

For example decimal seven requires that the 1, 2, and 4 bit lines be up. The 2 and 4 bits are AND gated (and inverted in the process) the 1 bit is simply inverted. A NOR gate is used which requires both inputs low for high output.

## 6.7 SCAN IN CIRCUIT (Dwg. #21494-7-1)

### General

The scan in circuits is composed of three sections, the strobe gates, the scan in gates and the four bit shift register. The scan in circuit is used to load the accumulator with data from the received code.

### Shift Register

Four flip-flop are connected to form a non-recirculating shift register. Refer to Figure 6.1 for the timing of the various signals.

The serial ONES line from the received code in connected to the "D" input of the first flip-flop, A30-5. The Q output feeds the 8 bit inputs of the three divide by 10 counters via inverting gates. In this way when a serial ONE is present, A30-5 will have a low output at Q which will be inverted before it is loaded into a divider. Since the $\overline{Q}$ output of A30-5 feeds A30-9, it is necessary to use the $\overline{Q}$ output from A30-9, A29-5 and A29-9 to maintain proper polarity.

The operation of the shift register is as follows:

The clock lines of all four flip-flops are energized once each 10 ms by the shift line. This causes the Q output to assume the same state as the "D" input. The shift register runs continuously and its outputs are strobed into the appropriate counter at the correct time.

### Strobe Gates

The strobe circuits for loading the three divide by ten stages are identical, only the times are different. Refer to the IRIG B time code format. At an index count of five (Y0, X5), the register will contain (from left to right) the 8 bit, 4 bit, 2 bit, and 1 bit for unit seconds. Therefore, gate A12-8, which strobes the unit seconds decade has as its inputs the X5 time, Y0 time and the scan in enable from the error bypass.

Similarly, at an index count of 14 the register will contain unit minutes information and gate A12-12 will strobe the unit minutes decade at X4, Y1 time. The unit hours will be strobed at X4, Y2 time (index count of 24).

The tens of seconds counter is strobed at X0, Y1 time. At this time the first flip-flop in the register does not con-

tain any code information. Note that A3, the tens of seconds decade, has no connection to A30-5 output.

The tens of minutes counter is strobed at X8, Y1 time. In this case the last flip-flop does not contain code information and there is no connection between it and A7.

Tens of hours is strobed at S8, Y2 time. Neither the first nor the last flip-flop of the shift register contain code information and, therefore, are not used by the tens of hours flip-flops.

### Scan In Gates

Each input to a counter has a control gate associated with it. This gate is enabled only in the Read Mode, thus preventing scan in at other times. Diodes are used to allow preset, where used.

## 6.8 ERROR BYPASS (Dwg. #21494-7-1)

### General

The error bypass circuit permits inhibiting scan in of information unless three sensecutive bad frames are received. With good data being received, the accumulators are updated by the EC signal.

### Error Detector

Gates A40-3, A40-6, and A40-8 form an exclusive OR gate. The $\overline{\text{SERIAL ONES}}$ from the scan out of the accumulators is compared to the $\overline{\text{SERIAL ONES}}$ from the received code. As long as both are the same, the input to A40-11 will be high. Should a difference exist, the input to A40-11 will go low. Gate A39-6 is necessary for two reasons. First, since the Model 8350 does not generate DAYS data, any DAYS information in the received code would appear to be an error. The input on pin 4 of A39-6 (from A39-8) will enable the gate only during the first 300 ms of the frame (when seconds, minutes and hours data is present). Second, duty cycle of the received $\overline{\text{SERIAL ONES}}$ and the internal $\overline{\text{SERIAL ONES}}$ is not the same. The input on pin 3 of A39-6 enables the gate during a time when both are present. Thus, only actual errors will cause A39-6 to go low.

### Error Flip-Flop

Flip-flops A37-5 and A37-9 will accumulate up to a count of three and are used to store the number consecutive bad frames. The input of A37-5 is clocked once each frame by the output of A31-5. Flip-flop A31-9 will be set by A31-5 once per frame. If no errors are present, A31-9 will remain set, enabling gate A38-6. Under this condition A37-5 and A37-9 will receive a clear signal with each clock signal, keeping both their outputs low. When an error is present, A31-9 will be reset prior to the clock pulse

for A37-5. Therefore, A37-5 will count ONE. If the error is still present in the next two frames, both A37-5 and A37-9 outputs will be up (count of three). These two outputs, and the four bit from the Z counter will produce enable signals to allow scanning in the next frame.

When the Mode switch is in other than the READ position, A31-9 is held set, preventing A37-5 and A37-9 from counting. Also, inverter A42-2 holds the enable line low, preventing scan in. Grounding the error bypass DEFEAT will hold both A37-5 and A37-9 outputs high causing every frame to scan in.

## 6.9 SCAN OUT GATES (Dwg. #21494-7-1)

### General

A series of gates is used to form the SERIAL ONES from the outputs of the counters in the Time-of-Day Accumulator.

### X Time Gates

Each Counter has a set of gates (one for each output needed) which are enabled by the X times. In this way, each output bit will be properly positioned in the serial code when the Y times are used to further select the outputs of the X time gates. For example, the bits from the unit seconds counter are inserted in the code at X1, X2, X3, and X4 times (during Y0 time). Therefore, gates A14 will output these bits when they are enabled by the X times.

### Y Time Gates

All X time outputs which will occur in the same Y time are connected to a Y time gate via an inverter. In this way, during a particular Y time, the various code bits which are associated with that segment of the code will appear as ONES or ZEROS on the $\overline{\text{SERIAL ONES}}$ line.

## 6.10 DC CODE GENERATOR (Dwg. #21494-7-1)

### General

A DC level shift code is produced from the SERIAL ONES generated by the scanout gating system. The code generator supplies correct width pulses to identify MARKS, ONES, and ZEROS. Refer to Figure 6.1.

### Pulse Terminating Gates

A series of gates is used to control the width of the output pulses. Gate A53-6 combines the inverted 1 bit and the 8 bit from the Z counter to produce a negative going transition 8 ms after the negative going transition of the X counter 1 bit. A54-6 will produce a negative transition 5 ms following the X counter 1 bit (from the Z counter 1 and 4 bits), unless either the $\overline{\text{X9}}$ or $\overline{\text{X0}\cdot\text{Y0}}$ lines are low. In this way no transitions are produced during the MARKS (X9 time is the regular MARK, X0$\cdot$ Y0 time is the extra MARK at the start

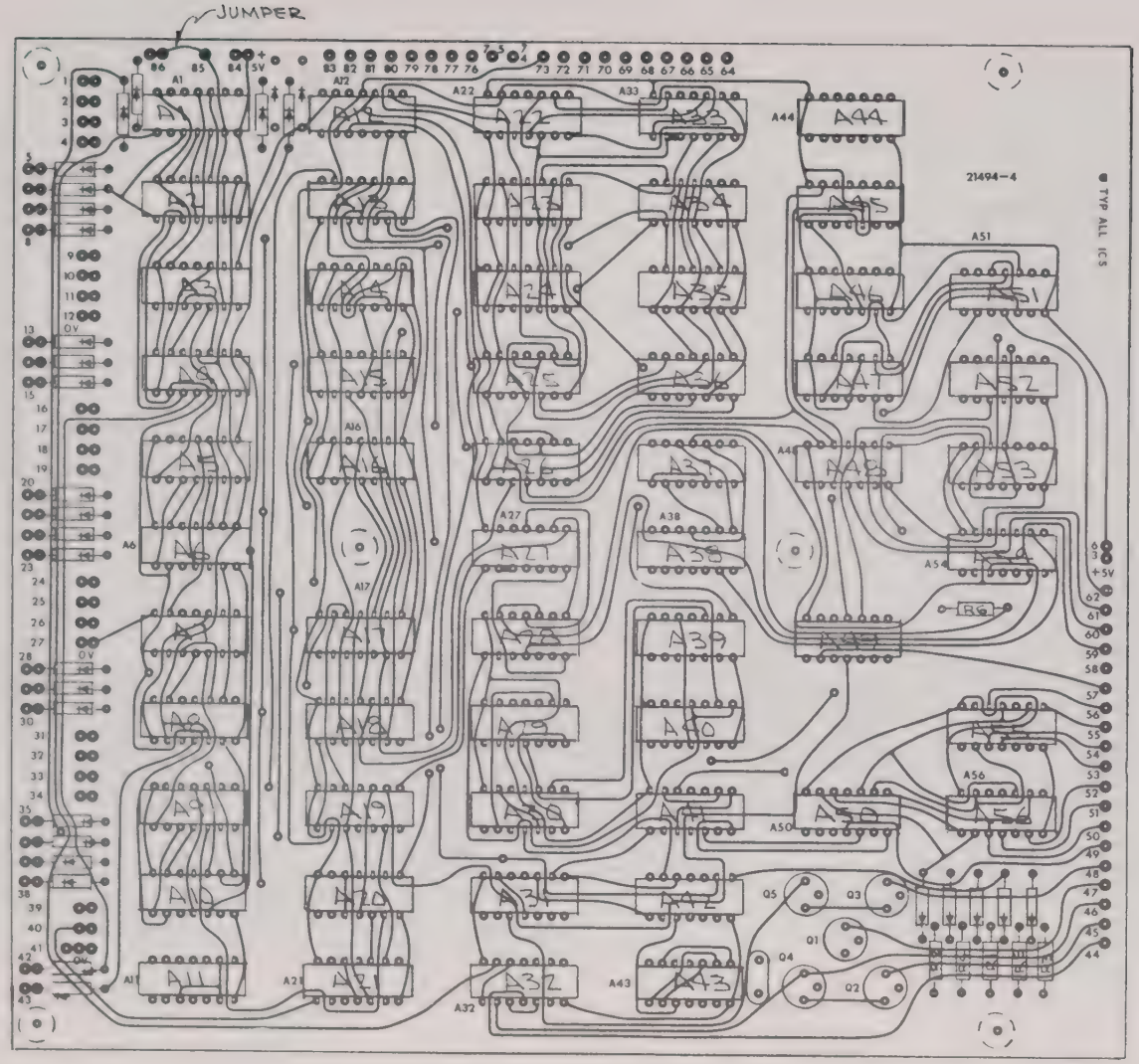
of each frame). Similarly A54-8 produces a negative transition 2 ms after the X counter 1 bit from the Z counter 2 bit) except during MARKS or when the $\overline{\text{SERIAL ONES}}$ line is low (indicating a ONE is to be inserted in the code).

### Code Flip-flop

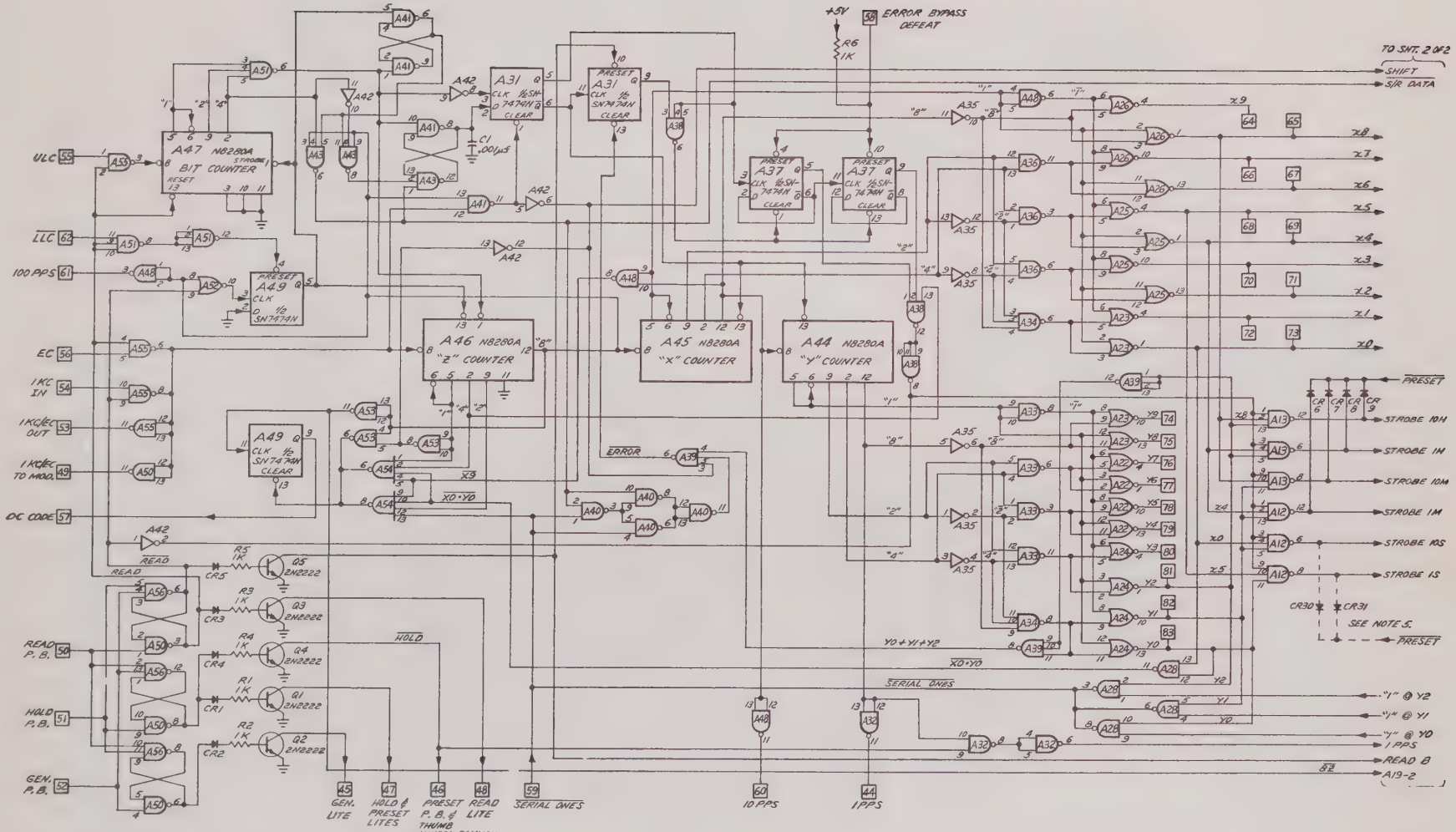
A49-9 is set, on time, once each 10 ms by the inverted 100 pps (Z counter 8 bit). It is cleared at the first negative transition of the width gates. Any subsequent pulses on the clear line have no effect. Thus, for a MARK the output of A49-9 is high for 8 ms (A54-6 and A54-8 stay up and A53-6 goes low at 8 ms); for a ONE the length is 5 ms (A54-8 stays up and A53-6 goes low at 5 ms); for a ZERO the length is 2 ms (A54-8 goes low at 2 ms).

## PARTS LIST

| Reg. | Description | Part No. |
|---|---|---|
| | Assembly | 21494-4-1 |
| | Schematic | 21494-7-1 |
| A1,5,9 44-47 | IC 8280A | 25722 |
| A2,4,6, 8,10,11 14-19,28 32,33,36 40,41,48 53,55 | IC 846N | 19716 |
| A3,7 | IC C2125A | 25723 |
| A12,13 34,38 39,43 51 | IC 862N | 19719 |
| A20,27 35,42 | IC 836N | 25704 |
| A21,29- 31,37 49 | IC 7474N | 25241 |
| A22-26 52 | IC 7402N | 25709 |
| A50 | IC 7400N | 19705 |
| A54 | IC 844N | 19714 |
| A56 | IC 7410N | 19706 |
| C1 | Capacitor 0.001 µf 500 V 20 % | C0424 |
| CR1-9, 12-31 | Diode IN4151 | CR0150 |
| R1-6 | Resistor 1 kΩ 1/4 W 5% | R0765 |
| Q1-5 | Transistor 2N2222 | Q0116 |




ASSEMBLY
LOGIC BOARD
MODEL 8350 IRIG B
21494-4-1 A

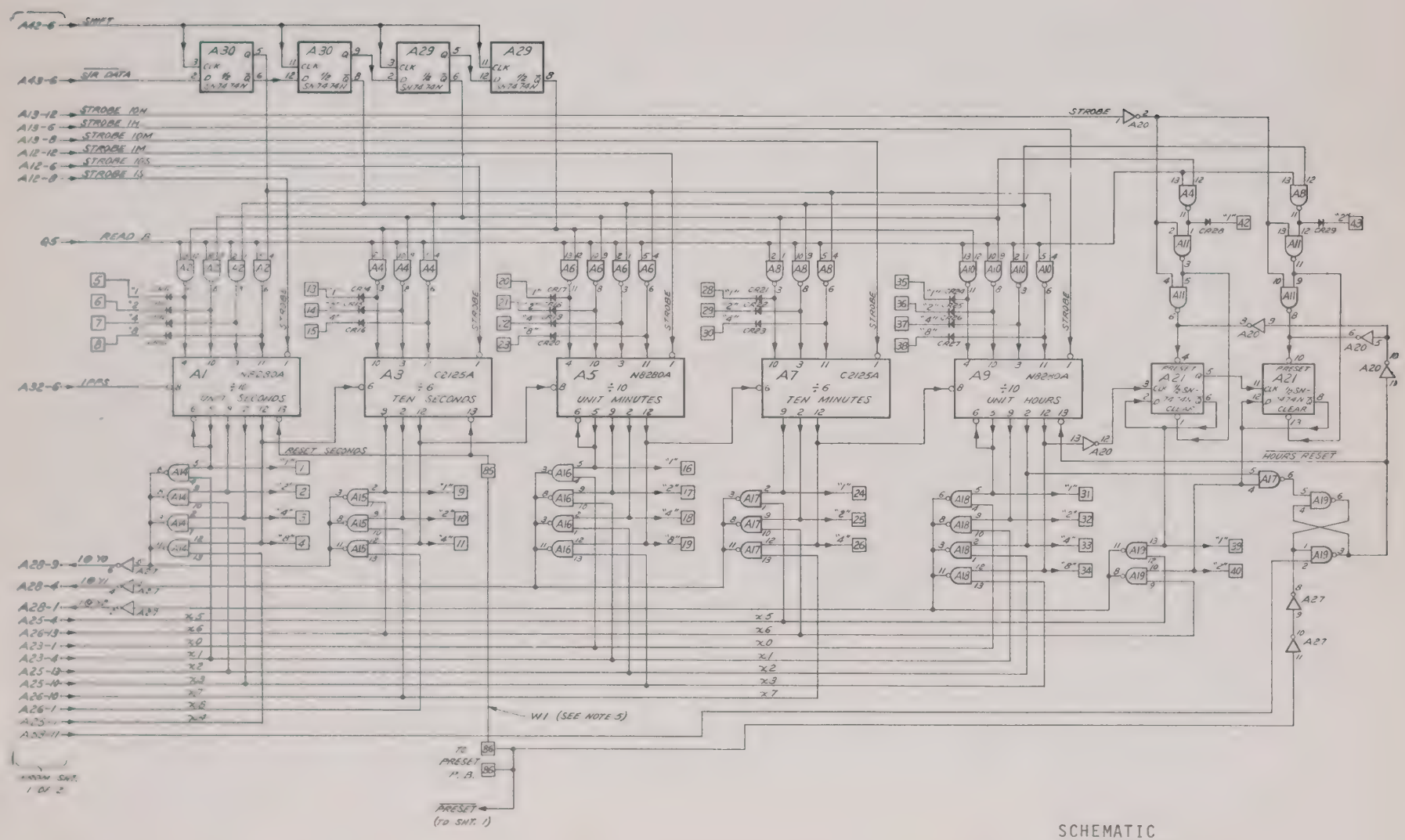



NOTES: UNLESS OTHERWISE SPECIFIED;
1. RESISTORS: ½ W, 5%, C.C.
2. DIODES: IN4151.
3. ALL I.C.'S PIN 7 IS CONNECTED TO GRD.
4. ALL " PIN 14 " " " "Vcc.
5. TO PRESET SECONDS, REMOVE W1 (SNT. 2) & ADD CR30 & CR31.

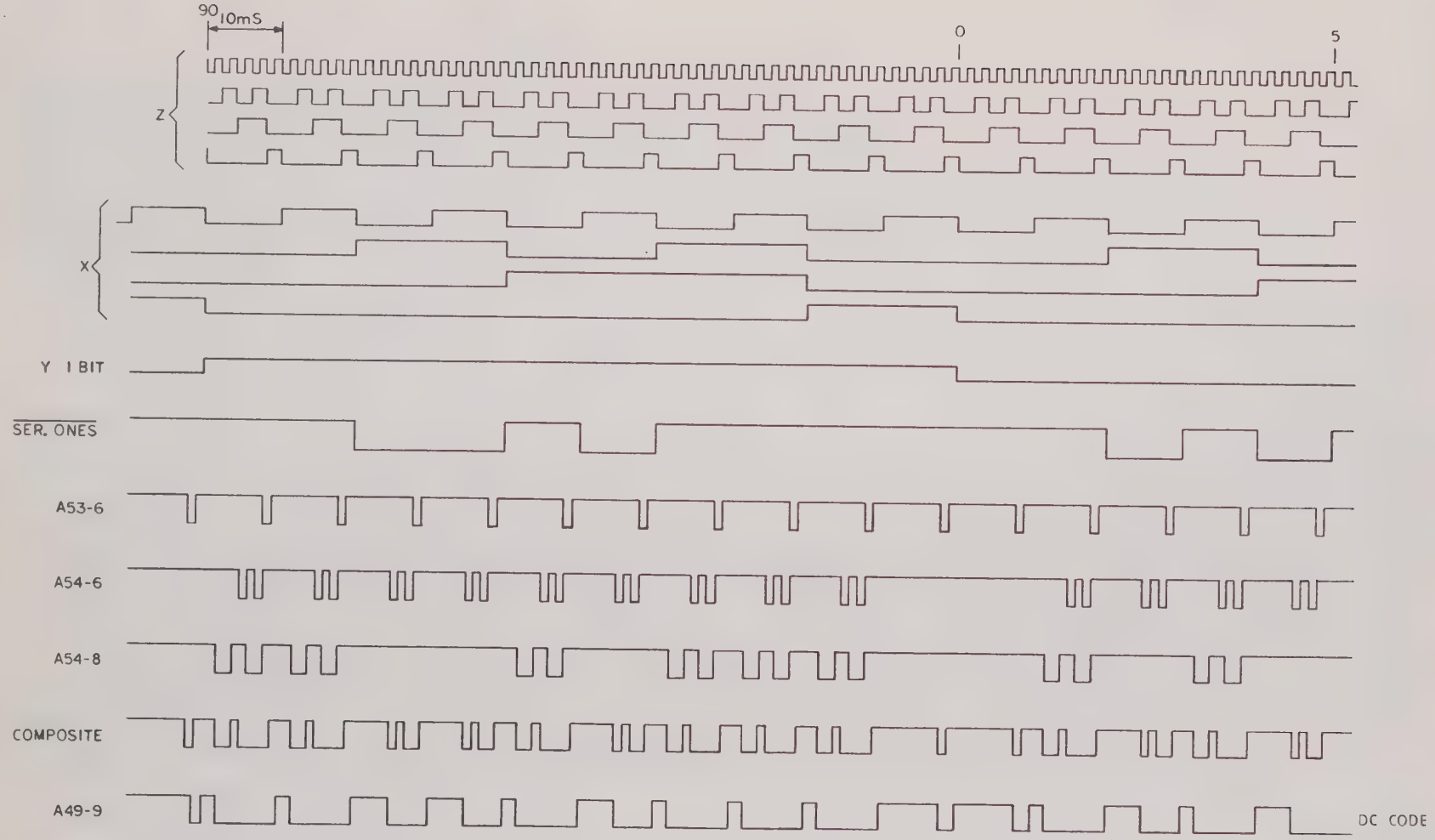
NOTES: (CONT.)
6. SN158486N - A2, A4, A6, A8, A10, A11, A14, A15, A16, A17, A18, A19, A28, A32, A33, A36, A40, A41, A48, A53, & A55.
SN158626N - A12, A19, A34, A38, A39, A43, & A51.
MC836P - A20, A27, A35 & A42.

SN7402N - A22, A23, A24, A25, A26, & A52.
SN7400N - A50.
SN158644N - A54.
SN7410N - A56.

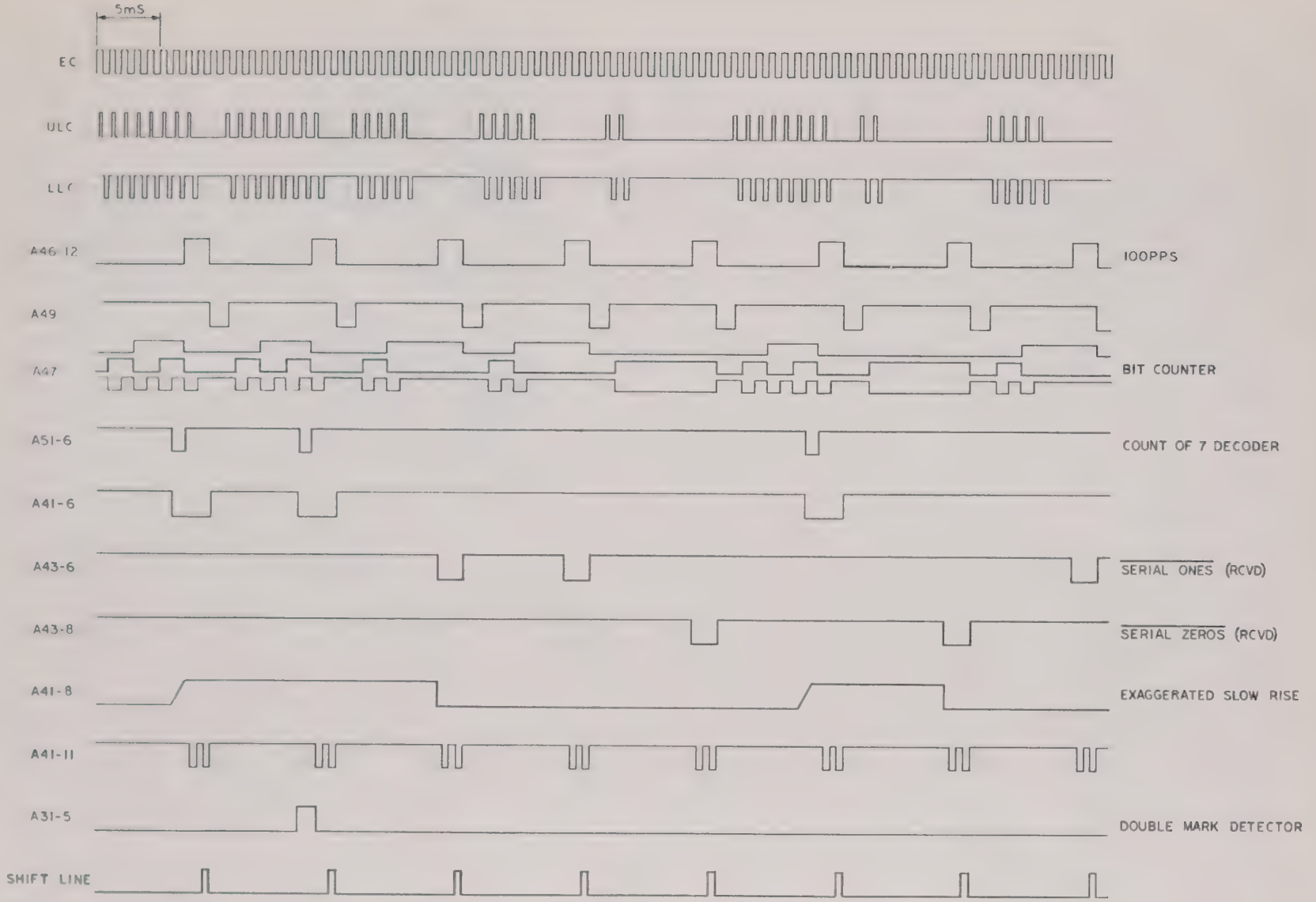
SCHEMATIC
LOGIC BOARD
MODEL 8350 IRIG B
21949-7-1 B Sh. 1




SCHEMATIC
LOGIC BOARD
MODEL 8350 IRIG B
21494-7-1 B Sh. 2




TIMING DIAGRAM
MODEL 8350 IRIG B
31422-7-1 Sh. 1
FIGURE 6.1




TIMING DIAGRAM
MODEL 8350 IRIG B
31422-7-1 Sh. 2
FIGURE 6.2

## 6.11 OSCILLATOR DECADE (Dwg. #21343-7-1)

### General

This assembly contains a 1 MHz oscillator and three integrated circuit decade dividers to produce a 1 k pps signal.

### Oscillator/Buffer

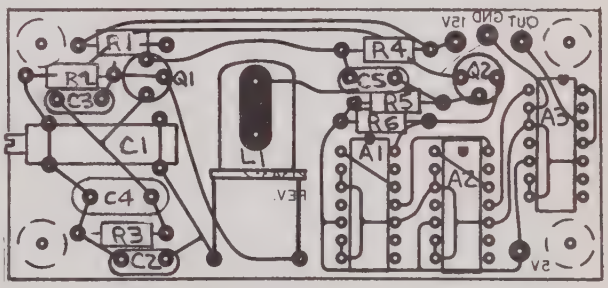
An unheated crystal, Y1 and feedback amplifier Q1 produce the 1 MHz reference signal. Transistor Q2 provides isolation to prevent loading of the oscillator.

### Decade Dividers

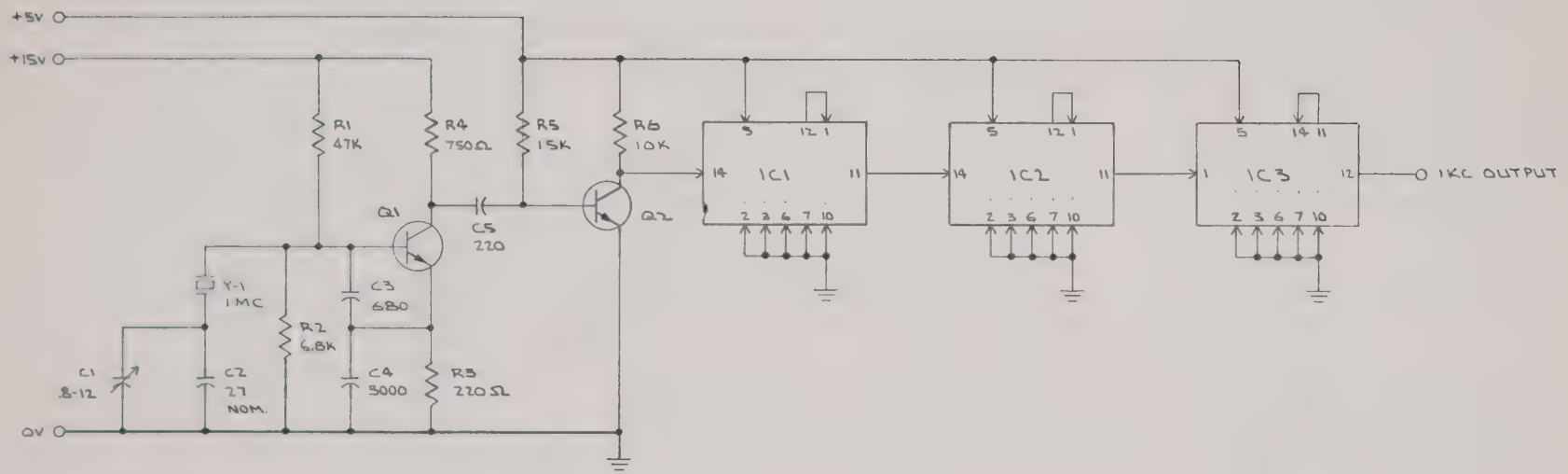
The 1 MHz signal from Q2 is successively divided by ten to produce the 1 kHz output. Dividers IC 1 and IC 2 are connected to divide-by-two-then-by-five. Divider IC 3 is a divide-by-five-then-by-two, producing a squarewave 1 kHz output.

PARTS LIST

| Ref. | Description | Part No. |
|---|---|---|
| | Assembly | 21343-4-1 |
| | Schematic | 21343-7-1 |
| C1 | Capacitor 0.8-12 (JFD VC31GW) | |
| C2 | Capacitor 27 pf 500 V | C0530 |
| C3 | Capacitor 680 pf 500 V | C0638 |
| C4 | Capacitor 3000 pf 500 V | C0759 |
| C5 | Capacitor 220 pf 500 V | C0538 |
| IC1-3 | IC SN7490N | 19711 |
| Q1,2 | Transistor 2N2222 | Q0116 |
| R1 | Resistor 47 kΩ 1/4 W ±5% | R0777 |
| R2 | Resistor 6.8 kΩ 1/4 W ±5% | R0696 |
| R3 | Resistor 220Ω 1/4 W ±5% | R0760 |
| R4 | Resistor 750Ω 1/4 W ±5% | R1425 |
| R5 | Resistor 15 kΩ 1/4 W ±5% | R0728 |
| R6 | Resistor 10 kΩ 1/4 W ±5% | R0766 |
| Y1 | Crystal 1 MHz | Y0019 |




ASSEMBLY
OSCILLATOR
DECADE BOARD
21343-4-1




NOTES

1- ALL RESISTOR VALUES IN OHMS, ¼w, 5%.
2- ALL CAPACITOR VALUES IN PF.
3- ALL TRANSISTORS 2N2222.
4- ALL IC'S SN7490N.

SCHEMATIC
OSCILLATOR
DECADE BOARD
21343-7-1

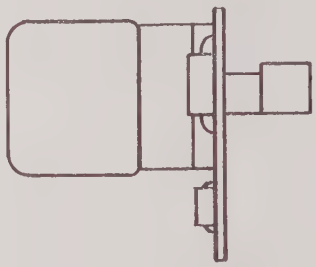
## 6.12 DISPLAY BOARD (Dwg. #21332-7-1)

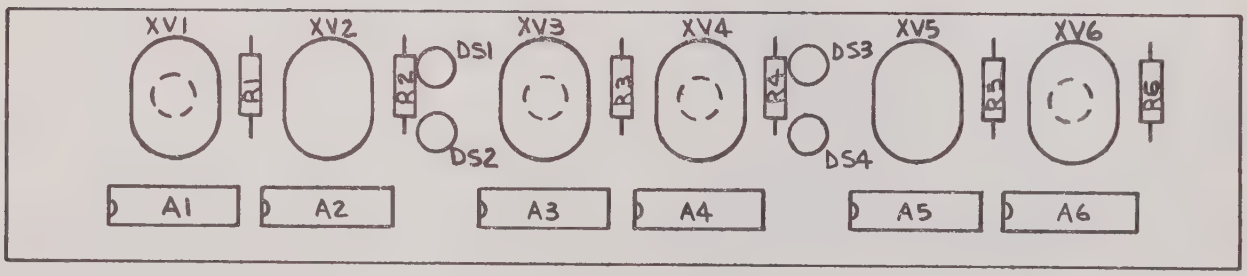
### General

The readout consists of six display tubes, with decoder/dividers and neon lamp colons. Each digit uses an integrated circuit to convert BCD information to decimal output. The decoders are capable of directly controlling the neon type display tubes.

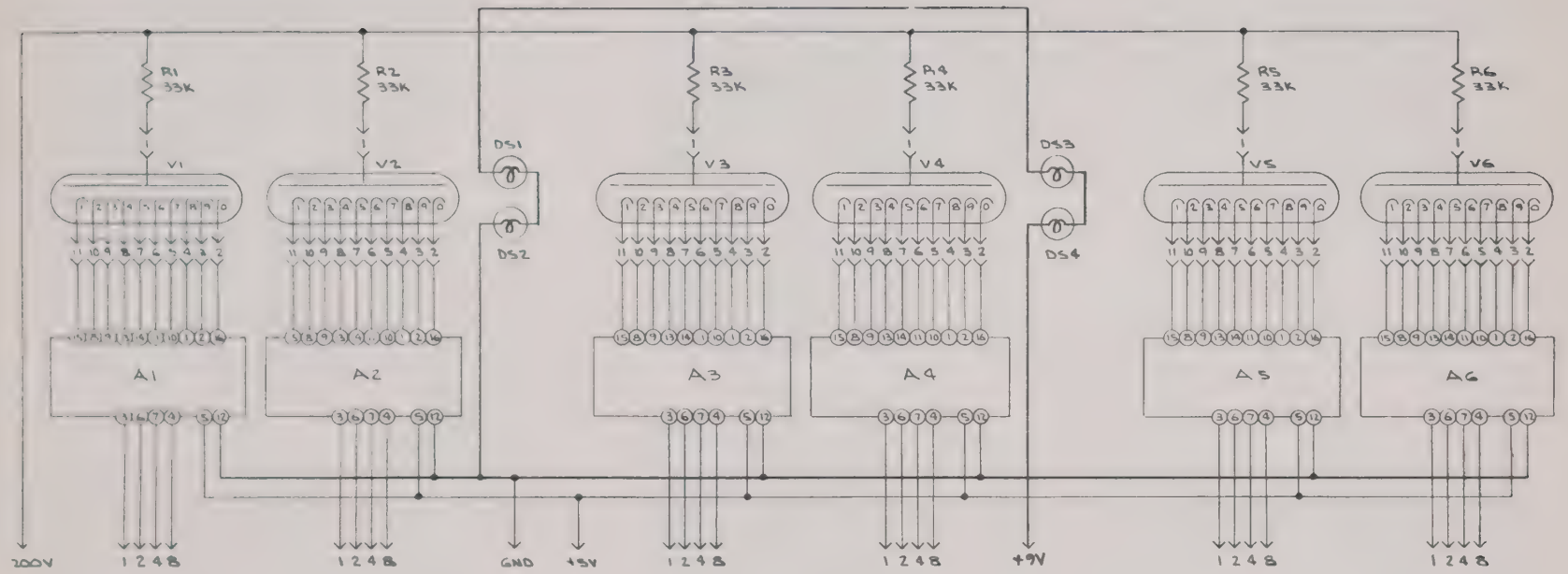
PARTS LIST

| Ref. | Description | Part No. |
|---|---|---|
| | Assembly | 21332-4-1 |
| | Schematic | 21332-7-1 |
| DS1-4 | Lamp Incandescant Chicago Min Lamp CM8-666 | 10050 |
| R1-6 | Resistor 33 kΩ 1/2 W 5% | R0262 |
| XV1 | Socket Tube (SK144A) IC SN744IN | 19707 |






ASSEMBLY
DISPLAY BOARD
21332-4-1 D




NOTES

1- A 1-6 ARE SN7441N
2- V1-6 ARE B5991
3- R1-6 ARE ½W ±5% COMP CARBON.

SCHEMATIC
DISPLAY BOARD
MODEL 8350
21332-7-1 D

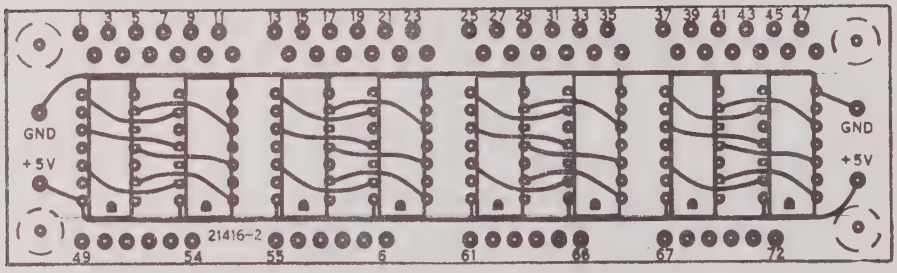
## 6.13 BCD OUTPUT OPTIONAL (Dwg. #21416-7-1)

### General

Eight integrated circuit hex inverters are used to provide buffers for twenty-four output lines. Each line is double inverted, with both the inverted and non-inverted (double inversion) outputs available. Output is 5 V logic level (DTL: 5 volt 6 kΩ source, 0 volts 15 mA sink).

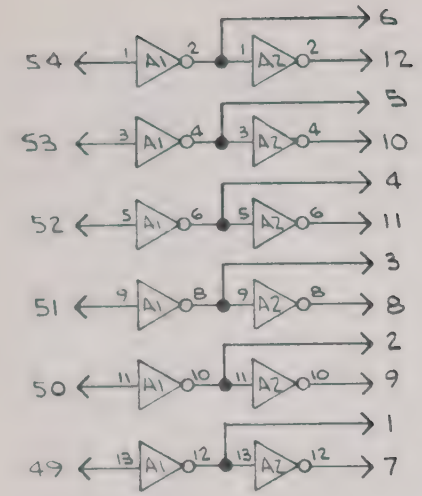
### PARTS LIST

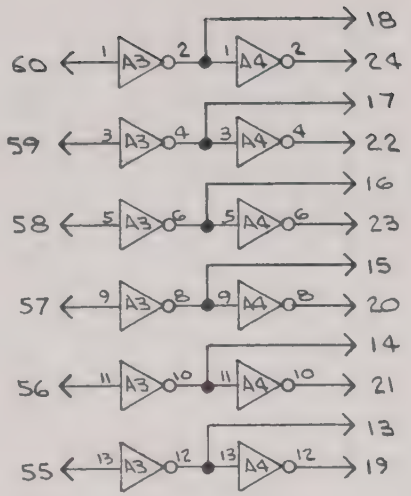
| Ref. | Description | Part No. |
|---|---|---|
| | Assembly | 21416-4-1 |
| | Schematic | 21416-7-1 |
| A1-8 | IC (836) | 25704 |
| | Standoff, CTC1247-9 | E0224 |



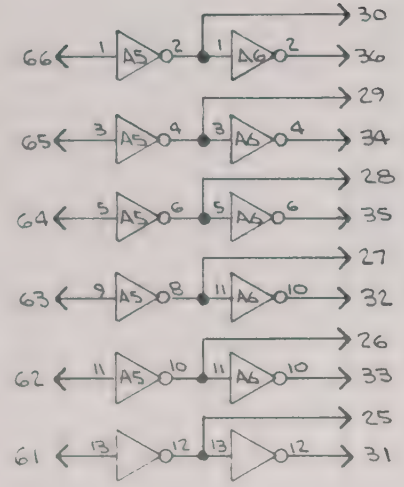

ASSEMBLY
BCD OUTPUT
21416-4

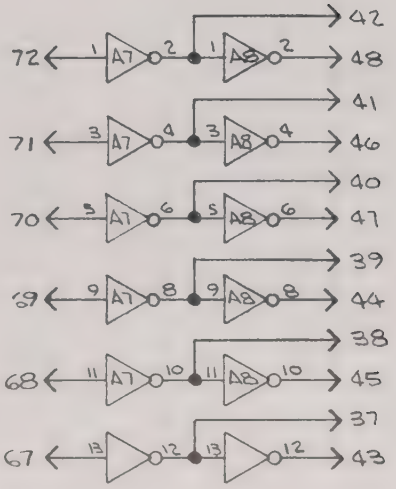
8350-11-69




NOTES:
1- ALL IC ARE TYPE 836
PIN 7 IS GND
PIN 14 IS +5V




SCHEMATIC
BCD OUTPUT
21416-7-1

## 6.14 INPUT OUTPUT BOARD (Dwg. #21940-7-1 or -3)

### General

This assembly provides two functions. One circuit demodulates a received code to extract the EACH CYCLE, LOWER LARGE CYCLE and UPPER LARGE CYCLE signals. The modulated code output of the Model 8350 is produced by another circuit.

### AGC Circuit

One portion of the input circuit contains a circuit to reproduce code at a predetermined amplitude by means of an AGC loop. The received code is applied to a voltage divider network composed of R18 and FET Q7. Q5 is operated as a source follower to raise the input impedance of amplifier IC 2 and, therefore, reduce loading of the voltage divider network.

Amplifier IC 2 operating as an inverting amplifier, has negative feedback to provide a controlled gain of 1000 via R20 and R23. A roll-off network (C13 and R24) insures stablity.

The amplified code is applied to the base of Q9, which is emitter coupled to Q8 and Q9 form a signal peak detection circuit which provides the AGC control voltage to the gate of Q7. Transistor Q6 is a constant current source which, in conjunction with C11 provides the AGC time constant. Potentiometer R37 allows adjusting the code level at the output of IC 2. The correct level is between 2 V and 3 V peak-to-peak.

### Cycle Detectors

The remaining three integrated circuit amplifiers, IC-3 thru IC-5 are used as cycle detectors. All three cycle detectors are driven in parallel from the AGC controlled amplifier.

IC 3 is a Schmitt trigger biased such that it will trigger at zero axis crossing, thus generating a squarewave at the input carrier frequency. The trigger point is adjusted with R40.

IC 4 and IC 5 generate output pulses only upon receipt of a large cycle. IC 4 is biased to trigger low when the code input reaches approximately 70% of a large cycle (in the negative direction). Note that IC 2 inverts the code, so the actual input to IC 4 is positive at the trigger. IC 5 triggers similarly (high) with a positive direction code cycle. Both IC 4 and IC 5 terminate their output pulses prior to the next zero crossing. The trigger points are adjustable by means of (lower) potentiometer R44 and (upper) potentiometer R48.

### Sine Wave Shaper

A 1 k pps signal on pin 5 is integrated by R1 and C2 and applied to the base of

constant current amplifier Q2. Q1 is an amplifier with C5 providing capacitive feedback. With capacitive feedback, the output (at R5) of this amplifier appears as an inductive reactance. The addition of C4 gives the circuit the electrical properties of a tuned tank circuit, with R5 used for phase adjustment. The signal at the gate of buffer amplifier Q3 is a sine wave which is fed to the modulator, Q4.

**Modulator and Output Amplifier**

The dc code is applied to the gate of Q4, causing the resistance of Q4 to vary. This variation changes the ratio of voltage divider R10, R12, R13, R14 producing an amplitude modulated code on a 1 kHz carrier. Potentiometer R13 permits varying the MARK TO SPACE ratio from 2:1 to 6:1.

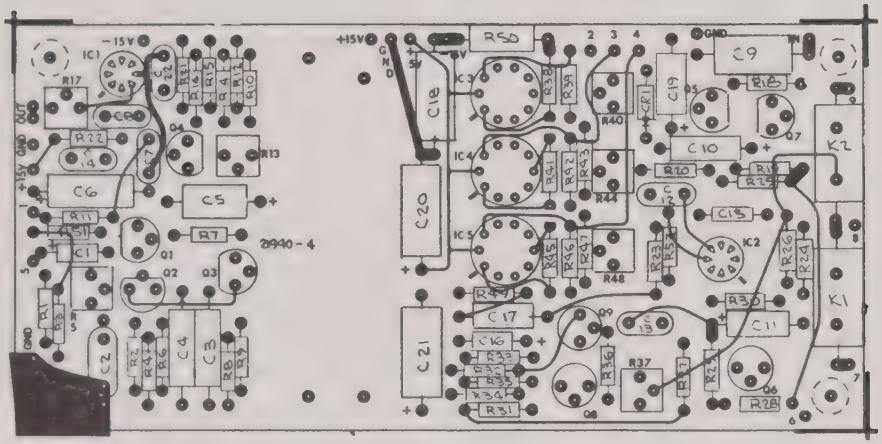
Amplifier IC 1 incorporates feedback which permits setting the gain of the amplifier and, therefore, the output level of the code. R17 allows adjustment from ZERO to 10 V pp.

PARTS LIST

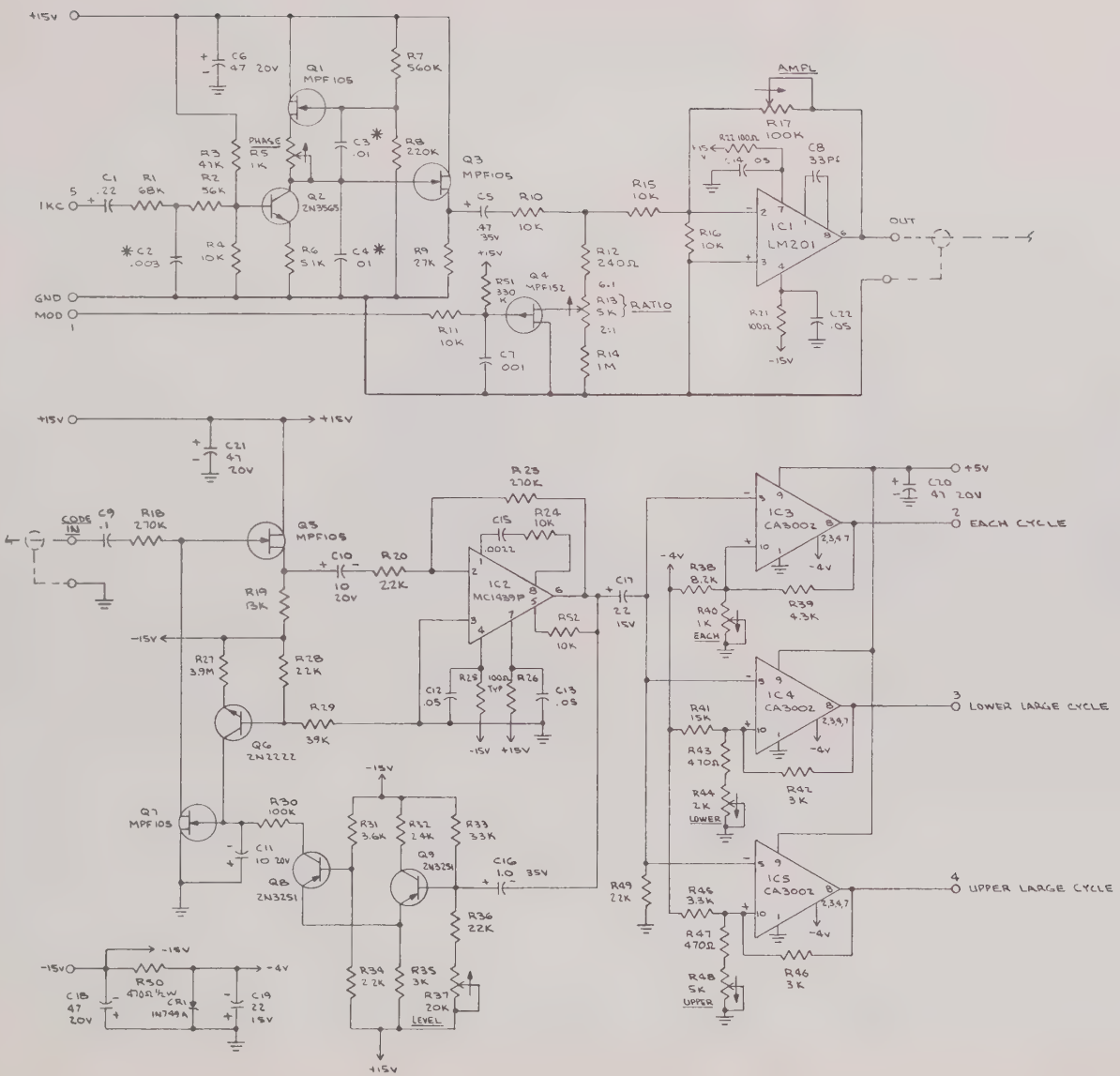
| Ref. | Description | Part No. |
|---|---|---|
| | Assembly | 21940-4-1 |
| | Schematic | 21940-7-1 |
| C1 | Capacitor 0.22 µf 10% 35 V | C0354 |
| C2 (-3) | Capacitor 0.015 pf 100 V | C0737 |
| C2 (-1) | Capacitor 3000 pf 5% 500 V | C0759 |
| C3,4 (-1) | Capacitor 0.01 µf 10% 50 V | C1000 |
| C3,4 (-3) | Capacitor 0.039 100 V CTM 393 VAK | C1184 |
| C5 | Capacitor 0.47 µf 10% [illegible] | C0733 |
| C6,18 20,21 | Capacitor 47 µf 10% 20 V | C0924 |
| C7 | Capacitor 0.001 DISC CER | C0235 |
| C8 | Capacitor 33 pf 10% 500 V | C0531 |
| C9 | Capacitor 0.1 µf 10% 200 V | C0987 |
| C10,11 | Capacitor 10 µf 10% 20 V | C0920 |
| C12,13 14,22 | Capacitor 0.05 DISC CER | C0672 |
| C15 | Capacitor 0.0022 µf | C0913 |
| C16 | Capacitor 1 µf 10% 35 V | C0524 |
| C17,19 | Capacitor 22 µf 10% 15 V | C1015 |
| CR1 | Diode IN749A | CR0306 |
| IC1 | IC (National LM201) | 25700 |
| IC2 | IC (Mot MC14396) | 25729 |
| IC3-5 | IC (RCA CA3002) | 25701 |
| R1 | Resistor 68 kΩ 1/4 W 5% CC | R0891 |
| R2 | Resistor 56 kΩ 1/4 W 5% CC | R1235 |
| R3 | Resistor 47 kΩ 1/4 W 5% CC | R0777 |
| R4,10, 11,15, 16,24 52 | Resistor 10 kΩ 1/4 W 5% CC | R0766 |
| R5,40 | Potentiometer 1 kΩ IRC Model 300 | |
| R6 | Resistor 5.1 kΩ 1/4 W 5% CC | R0693 |
| R7 | Resistor 560 kΩ 1/4 W 5% CC | R1321 |

| Ref. | Description | Part No. |
|---|---|---|
| R8 | Resistor 220 kΩ 1/4 W 5% CC | R0967 |
| R9 | Resistor 2.7 kΩ 1/4 W 5% CC | R0937 |
| R12 | Resistor 240Ω 1/4 W 5% CC | R0835 |
| R13,48 | Potentiometer 5 kΩ Bourns 330 P-1-502 | R1545 |
| R14 | Resistor 1 M 1/4 W 5% CC | R0962 |
| R17 | Potentiometer 100 kΩ IRC Model 350 | |
| R18,23 | Resistor 270 kΩ 1/4 W 5% CC | R1622 |
| R19 | Resistor 0.13 kΩ 1/4 W 5% CC | R0882 |
| R20 34,49 | Resistor 2.2 kΩ 1/4 W 5% CC | R0749 |
| R21,22 25,26 | Resistor 100Ω 1/4 W 5% | R0966 |
| R27 | Resistor 3.9 MΩ 1/4 W 5% CC | R1578 |
| R28,36 | Resistor 22 kΩ 1/4 W 5% CC | R0768 |
| R29 | Resistor 39 kΩ 1/4 W 5% CC | R0748 |
| R30 | Resistor 100 kΩ 1/4 W 5% | R0741 |
| R31 | Resistor 3.6 kΩ 1/4 W 5% CC | R0938 |
| R32 | Resistor 2.4 kΩ 1/4 W 5% CC | R1045 |
| R33 | Resistor 33 kΩ 1/4 W 5% CC | R0780 |
| R35,42 46 | Resistor 3 kΩ 1/4 W 5% CC | R0711 |
| R37 | Potentiometer 20 kΩ IRC Model 300 | |
| R38 | Resistor 8.2 kΩ 1/4 W 5% CC | R0883 |
| R39 | Resistor 4.3 kΩ 1/4 W 5% CC | R0702 |
| R41 | Resistor 15 kΩ 1/4 W 5% CC | R0728 |
| R43,47 | Resistor 470Ω 1/4 W 5% CC | R1044 |
| R44 | Potentiometer 2 KΩ IRC Model 300 | |
| R45 | Resistor 3.3 kΩ 1/4 W 5% CC | R0742 |
| R50 | Resistor 470Ω 1/2 W 5% CC | R0677 |
| R51 | Resistor 330 kΩ 1/4 W 5% CC | R1203 |
| Q1,3,5 7 | Transistor MPF105 | Q0264 |
| Q2 | Transistor 2N3565 | Q0237 |
| Q4 | Transistor MPF152 | Q0263 |
| Q6 | Transistor 2N2222 | Q0116 |
| Q8,9 | Transistor 2N3225I | Q0174 |
| | Standoff Swage CTC 1247-9 | E0224 |
| | Pad Milton-Ross #10050 | |

DETAIL A




ASSEMBLY
INPUT/OUTPUT
CIRCUIT
21940-4-1




NOTES-

1- ALL RESISTOR VALUES IN OHMS, 1/4W, 5%.

2- ALL CAPACITOR VALUES IN MFD.

G3 ASSY C2 = .015 MFD
C3 = .039 MFD
C4 = .039 MFD

SCHEMATIC
INPUT/OUTPUT
CIRCUIT G1 & G3
21940-7-1 A

## 6.15 OVERALL CHASSIS PARTS LIST

| Ref. | Description | Part No. |
|---|---|---|
| | Final Assembly | 31000-4-1 |
| | Power Supply Assembly | 19734 |
| | Auxillary Chassis Assembly | 23479 |
| | AC Line Cord | W0076 |
| | Display Board Assembly | 21332-4-1 |
| | OSC Decade Assembly | 21343-4-1 |
| | Input/Output Assembly | 21940-4-1 |
| | Logic Board Assembly | 21494-4-1 |
| | Standoff Insulated | E0098 |
| | Eyelet | E0088 |

### FRONT PANEL

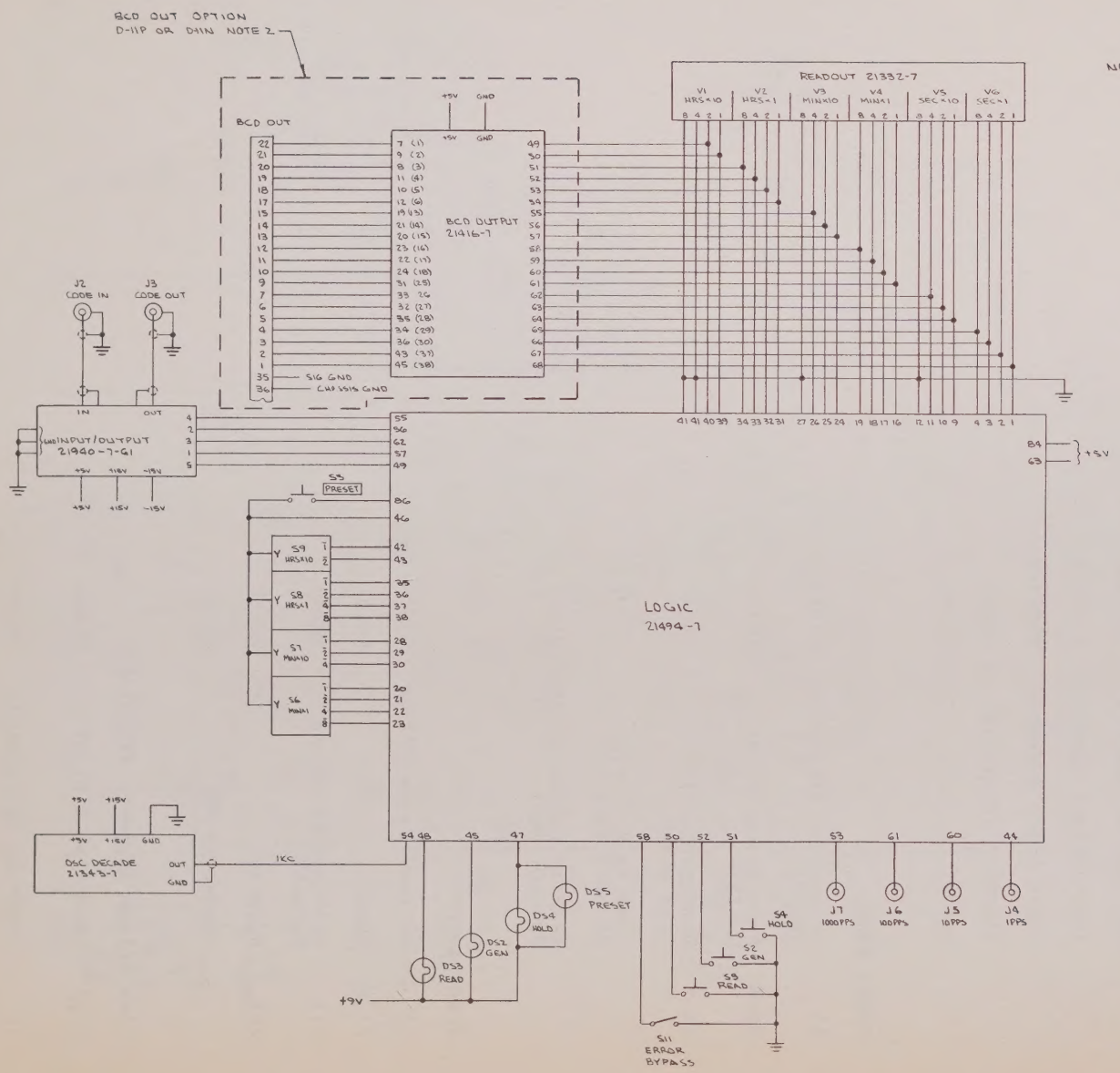
| | | |
|---|---|---|
| S1 | Pushbutton (Truco 01-221) | S0358 |
| S2-5 | Pushbutton (Truco 01-121) | S0357 |
| S6-9 | Switch Digitran Type 8794 | S0380 |
| | Lamp 12 V (Truco #01-903-12 V | I0081 |
| | Display Screen (Truco #01-901- NH) | H1811 |

### REAR PANEL

| | | |
|---|---|---|
| J1 | AC Input/Line Filter | 31331-4-1 |
| F1,2 | Fuse | F0001 |
| S11 | Switch SPST (Error Bypass) | S0149 |
| XF1,2 | Fusepost | X0034 |
| | Connector BNC | J0165 |

### Line Filter Assembly #31331-4-1

| | | |
|---|---|---|
| C1,2 | Capacitor 0.01 µf 500 V | C0423 |
| J1 | Reset AC Switchcraft | J0566 |
| L1,2 | Hash Filter (JW Miller #5250) | L0166 |
| | Terminal | E0141 |




NOTES

1- FOR POWER SUPPLY SEE 21374-7

2- PIN CONNECTIONS IN ( ) FOR NEG LOGIC D-11N OPTION

WIRING BLOCK DIAGRAM
MODEL 8350 IRIG B
31000-7-1 A

MP MASTER
MA34105